Test of the Inter-Connect-Boards

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Petals will be delivered to the integration centers with ICBs mounted, but without AOHs, CCUMs and DOHMs

All ICBs will be pin to pin electrically tested before mounting on petals

At startup of the production, functional tests of electrically equipped petals (5%-10%) foreseen in Aachen:
CMS like readout: electrical control link, 2 CCUMs, several FEH and AOHs, DAQ for T- and H-probes

Functional test of all petals after transport at integration centers prior to Si-Module assembly
InterConnectBoard (ICB)

ICB provides LV and HV, trigger/clock, reset and control signals to the devices on the petal, and transmits data from the FE-Hybrids to Opto-Hybrids.
Test of the Interconnect Boards

The ICB quality will be controlled after each stage of the production:

- After pcb production electrical test of the bare boards
- Micrograph analyze of each production lot
- Visual control after soldering at the industry
- Electrical tests after soldering at the industry
  Requirement: producer must be provided with test setup
- Visual and electrical test of all ICBs in Aachen after delivery
- Attributes to test:
  - functionality of CMOS/LVDS drivers
  - open pins
  - shorts
  - HV insulation
Test Setup

- PC controlled system, which is modular, based on:
  - Commercial Digital I/O cards with 160 Inputs and 160 Outputs
  - HV – Supply
  - Test Cables
  - Adapter cards individual for each ICB type
  - Test Software
Example: Test equipment for ICB46 FP
Test Software

Generates test pattern individually adapted for each ICB type
Records the signal level on all outputs of tested ICB simultaneously
Compares recorded data with the expected response
Informs user, where the faults are located: connector number, pin number, name of the net
Records leakage current from HV-supply
Generates and stores test protocols
| PCI#1, CN1: | 00000000000000000000000000000000 |
| PCI#1, CN2: | 00000000000000000000000000000000 |
| PCI#1, CN4: | 00000000000000000000000000000000 |
| PCI#1, CN5: | 00000000000000000000000000000000 |

**Failure(s): 4**

| /RST53 | CON57 1:54 | FE54:33 | /RST54 |
| PCI#1, CN2:62 | PCI#1, CN1:46 | Expected Level: 1 | (inv) |
| Actual Level: 0 | Actual Level: 0 |

| LU3VSS | CON57 1:39... | FE51:4... | LU3VSS |
| PCI#1, CN1:11 | Expected Level: 0 |
| Actual Level: 1 |

| /RST53 | CON57 1:54 | FE53:33 | /RST53 |
| PCI#1, CN2:62 | PCI#1, CN1:40 | Expected Level: 1 | (inv) |
| Actual Level: 0 | Actual Level: 0 |

| /RST51 | CON57 1:50 | FE52:33 | /RST52 |
| PCI#1, CN2:61 | PCI#1, CN1:6 | Expected Level: 1 | (inv) |
| Actual Level: 0 | Actual Level: 0 |
Status of the Test System

- the concept is validated
- designs of all Adapter Boards for Front Petal (10 different pcbs) ready
- boards are produced and assembled; test of the boards in progress
- designs of all Adapter Boards for Back Petal (10 different pcbs) ready
- test software is ready
- look up tables, data banks are generated
- test cables produced

**next steps**
- test of the Adapter Boards
- validation of the Test System
- After validation, reproduction of the system for the assembling company
In addition to the electrical test, a “functional test” with the CMS-like DAQ is planned for the first $\approx 10\%$ of ICBs in Aachen.

**Reasons:**
- check, if in electrical test all potential problems are found
- electrical test system checks only single boards, not the connections between the boards

The PIC must perform a reception test before mounting modules.

**Procedure:**
- The inserts are tested for **electrical insulation**
- The ICBs are screwed onto the petal
- With a hybrid and an AOH, **pedestals** are taken at each position of the board, using the **standalone** program
- ICBs are registered in the data base

!Caution: the **CCUMs** will be tested and distributed by CERN, not Aachen!
 Functional Test of the ICB

By testing the readout with standalone, we test:

- LV connections
- sense wire connections
- LVDS buffer functionality
- if the control ring is closed
- if the CCUs are found
- if the reset works
- if the I2C communication works for all positions
- if the timing signals arrive at each position
- if the data connection from FE-hybrid to AOH exists for all positions

If there is a problem (error message, no frame seen): debug with the scope! (and use debugger programs with the help of a physicist)

- **Time needed per petal: ca. 2 hours** (might use more hybrids at a later stage)
- Will be done by a technician (an ICB designer)

In addition: test of HV and temperature lines
Several 6APV hybrids with stiffener problem and a few AOHs are available for the testing.

These measures should assure that the equipment survives a significant number of tests.
Status:

Hardware requirements:
• FEC, FED, TSC, O-FED, VME crate, 2 CCUs, LV PS (one group is enough), digital power supply → everything is available.
• PC with DAQ: available in the system test setup
  ⇒ If necessary, could start immediately using the system test setup

In progress:
• installation of new version of DAQ software on a second PC
  ⇒ once this works, the old system test PC will be moved to the workshop and a setup installed there

To be done:
• Readout of temperature and humidity sensors via CCU and MS cable.