R&D at RWTH Aachen towards DC-DC Conversion Powering Schemes for the CMS Tracker at SLHC

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2nd Alliance Detector Workshop
Hamburg, April 2nd, 2009
• Motivation
• DC-DC conversion
• Noise studies
  – System test with CMS tracker modules
  – Converter noise spectra
  – Detector susceptibility
• Material budget analysis
• Summary & outlook
**Why is a new powering scheme needed?**

**SLHC**: increase of peak luminosity from $10^{34}\text{cm}^{-2}\text{s}^{-1}$ to $10^{35}\text{cm}^{-2}\text{s}^{-1}$ until ~ 2019

**Consequences for CMS silicon tracker power provision:**

- Number of charged particles in tracker increases by a factor of ~20
  - sensitive element size must decrease (occupancy) ⇒ more readout channels
- Tracker information to be incorporated into level-1 trigger to keep current trigger rate
  - track trigger layers with more complex readout electronics needed
- Front-end electronics deploys smaller feature size CMOS process (250nm → 130nm ...)
  - Savings in power/channel, but ...
  - ...lower operating voltage ⇒ higher currents ⇒ larger power losses ~ $I^2$
- Decrease of material inside the tracker is a main objective
- No space for additional power cables and no access to current services

⇒ A new powering scheme seems inevitable for the strip tracker.
Two technologies: Serial Powering and DC-DC conversion

→ CMS task force recommended **DC-DC conversion as baseline option** (Jan. 09)

Converter \( C \) converts a “high” DC input voltage to voltage needed by detector D \((V_0)\)

Conversion ratio \( r = \frac{V_0}{V_{in}} < 1 \)

⇒ Lower input currents and power losses: \( I_{in} = I_0 \cdot r \) & \( P_{drop} = R_{cable} \cdot I_0^2 \cdot r^2 \)

e.g. \( r = 1/10 \) ⇒ \( P_{drop} = 1/100 \)
DC-DC Converters

- Many technologies (inductor-based, capacitor-based...) and types exist
- Inductor-based converters provide large currents and are very efficient
  - R&D concentrates on buck converter as the simplest variant

\[ V_{in} \approx 12V \Rightarrow \text{HV-tolerant semi-conductor technology needed} \]
\[ \Rightarrow \text{radiation-hardness (CERN electr. group)} \]

\[ \text{Ferrites saturate for } B > ~2T \Rightarrow \text{air-core inductor needed} \]

\[ \text{bulky} \]
\[ \text{radiates noise} \]

\[ \text{Switching noise} \]

\[ \text{Efficiency} \]
\[ \text{Material budget} \]
\[ \text{Space constraints} \]
• Commercial buck converters used to systematically investigate effects on CMS FE-electronics (custom converters still in early prototyping phase)

• Enpirion EN5312QI & EN5382D: $f_s = 4\text{MHz}$, $V_{in} < 7\text{V}$, $I_{out} = 1\text{A}$

• Each silicon module is powered by 2 buck converters (1.25V, 2.50V)

• Many PCB variants: ferrite/air-core inductor, solenoid/toroid, Low DropOut reg., ...
System-Test Set-Up

- A lot can be learned from current CMS tracker hardware
- Move to SLHC readout chips and module prototypes asap - not before 2010

CMS Silicon Strip Petal

Ring 6 modules

Motherboard

Converter PCB

FE-hybrid with 4 APV25 chips:
- 128 x pre-amplifier, CR-RC shaper, pipeline
- analogue readout
- 50ns shaping time

Raw noise of module 6.4 with "conventional" powering via PS.

Standard powering

Raw noise [ADC counts] vs Strip number
Results from System-Test

Note: edge strips noisier than others → on-chip Common Mode subtraction fails → see “real“ CM
⇒ Current FE-electronics is sensitive to conductive and radiated converter noise
⇒ With a combination of filtering and shielding noise increase is negligible
→ Improve PCB layout, develop efficient filtering and low mass shielding (ongoing)
→ Learn about converter noise and coupling mechanisms
Converter Noise

• Noise can be measured with active differential probe and oscilloscope ⇒ painful
• Spectrum analyzer needed to quickly measure complete noise spectrum

Internal ferrite inductor

6mV_{pp} 4 MHz ripple
9mV_{pp} high f ringing from switching edges

2mV/div 100ns/div

Active differential probe funded by HGF alliance – to be endorsed by MB
Electromagnetic Compatibility Test Set-Up

- Standardized test set-up for cond. Common & Differential Mode (CM/DM) noise
- Quick characterization & comparison of converters, indep. from detector system
- Enables comparisons betw. different institutes

Current probe funded by HGF alliance – to be endorsed by MB

LISN: Line impedance stabilization network; isolates DUT from PS

PS
Spectrum analyzer
Copper ground
Current probe
Converter
Load

Converter

LISN

Power Supply

DUT

Load

Spectrum Analyzer

Signal source
Noise source

CM

DM

Load

Signal source
Noise source
Stray capacitance
Reference ground surface
Low DropOut (LDO) Regulator

- Linear voltage reg. with small voltage drop
- Linear technology VLDO regulator LTC3026
- LDO reduces voltage ripple = DM noise
- Module noise significantly reduced
  → high sensitivity to DM mode noise

Effect of LDO with internal inductor

- No converter
- No LDO
- With LDO, dropout = 50mV

DM without LDO

- Peak: 29.09dB \( \mu \text{A} \)
- Peak: 17.87dB \( \mu \text{A} \)
- Peak: 12.21dB \( \mu \text{A} \)

DM with LDO

- Peak: 2.80dB \( \mu \text{A} \)
- Peak: 0.00dB \( \mu \text{A} \)
- Peak: 0.00dB \( \mu \text{A} \)
Air-Core Inductors

- Two noise structures specific for air-core coils:
  - “Wings”: decrease with shielding ⇒ radiation
  - “Combs”: decrease with LDO ⇒ conductive
- Increase of cond. noise confirmed by EMC set-up

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**External air-core solenoid**

- 1. Peak: 36.65dB μA
- 2. Peak: 30.10dB μA
- 3. Peak: 22.30dB μA

**Internal ferrite inductor**

- Quadr. Summe: 32.36dB μA
- 1. Peak: 29.09dB μA
- 2. Peak: 17.87dB μA
- 3. Peak: 12.24dB μA
- Correlation between module & converter noise clearly seen (but not 1)
- Both EMC test-stand and system test give valuable information
Noise Susceptibility vs. Frequency

- Study detector susceptibility vs. frequency to identify critical frequency bands
- Inductive injection of DM & CM sinus currents into cables (bulk current injection)

![Diagram of noise susceptibility setup]

- Power Supply
- LISN
- Sine Wave Generator
- Injection Probe
- Amplifier +50dB
- Current Probe
- Spectrum Analyzer
- CMS Petal

Amplifier funded by HGF alliance – to be endorsed by MB

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R&D towards a DC-DC Conversion Powering Scheme for the CMS Tracker
• Higher susceptibility to injection into 1.25V line (pre-amplifier reference voltage)
• Higher susceptibility to Differential Mode noise
• Expect peak at $1/(2\pi \cdot 50\text{ns}) = 3.2\text{MHz}$ from shaper
• **Broad peak at $\sim 6-8\text{MHz}$** ⇒ “system response“ measured rather than APV response
Coupling to Bias Ring

- Edge strips are noisier due to cap. coupling to bias ring
- Bias ring connected to 1.25V instead of ground \(\Rightarrow\) susceptibility decreases drastically
- Results specific to current module design, but set-up will be very useful once SLHC modules exist

![Graph showing noise levels vs. frequency](image)

APV25 pre-amplifier

- Bias ring referenced to ground
- Bias ring referenced to 1.25V

[Mark Raymond]
Powering scheme changes MB of
- Electronics (+ converter, - PCBs)
- Cables (inside the tracker)
- Cooling (local efficiency)

*Estimate MB for powering schemes*
- within the official software (CMSSW)
- for current tracker geometry
- focus on Tracker End Caps (TEC)

*Caveat: results can only be indicative!*
Assumptions:
r = 1/8
1 converter per module, on FE-hybrid

Simulated components:
- **Kapton substrate** (30mm x 33mm, 200μm)
- 4 copper layers (20μm each, 2x100%, 2x50%)
- **Toroid** (42 copper windings, plastic core)
- Resistors & capacitors
- **Chip** (Si, 3mm x 2mm x 1mm)
Savings in Cables and Motherboards

• Voltage drop \( dU \) between power supply and detector fixed to current maximal value
• Cable cross-section \( A \) for a given current \( I \):
  \[ A = \rho \cdot L \cdot I / dU \]

• Lower currents in PCBs if converter near module
• New PCBs “designed“
• Power loss required to be < 10%
MB for the TEC

TEC motherboards: -52.9%

TEC power cables: -65.7%

TEC electronics & cables: -27.3%

Total TEC MB: -7.5%

Original TEC MB

TEC with DC-DC conversion
Is it better to place the converters further outside?

⇒ Lower contribution from converter itself, but higher currents in motherboards

• Savings in electronics & cables: **21.6%** (cf. 27.3%)
• Total TEC savings: **6.0%** (cf. 7.5%)

⇒ Slight advantage for position near module
Serial Powering vs. DC-DC Conversion

**Implementation of SP** (inspired by Atlas talks):
- All modules of a petal powered in series
- Additional components per module:
  - chip, Kapton, bypass transistor, 6 capacitors and 3 resistors/chip for AC-coupling
- Power loss in motherboards !< 10%
- Cable cross-sections calculated as before

<table>
<thead>
<tr>
<th>Savings [%]</th>
<th>SP</th>
<th>DC-DC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power cables</td>
<td>72.4</td>
<td>65.7</td>
</tr>
<tr>
<td>Motherboards</td>
<td>51.6</td>
<td>52.9</td>
</tr>
<tr>
<td>Electronics &amp; cables</td>
<td>34.3</td>
<td>27.3</td>
</tr>
<tr>
<td>Total TEC</td>
<td>9.4</td>
<td>7.5</td>
</tr>
</tbody>
</table>

⇒ Serial Powering performs slightly better than DC-DC conversion
• **System-tests** with current tracker structures give valuable insight
• Bottom line: **with LDO, shielding and toroid coils noise increase is negligible**
• Need to move to SLHC prototypes asap – new readout chip expected for 2010

• Measurements of converter noise spectra with **EMC set-up** very useful
• Susceptibility set-up with **BCI** ready; automation needed for deeper understanding
• Scanning table to study inductive coupling in preparation

• **Material budget** analysis indicates possible improvement of the order of 7% for DC-DC conversion and 9% for Serial Powering

• Improvement of **PCBs**, shielding and coil design is ongoing
• Once tracker layout is converging, converter **integration** will get more concrete

Thanks to Prof. Lutz Feld (group leader), Dipl.-Ing. Waclaw Karpinski (PCBs), Rüdiger Jussen (EMC & BCI), Jennifer Merz (MB), Jan Sammet (system tests)
Back-up Slides
Open and Edge Channels

- 128 APV inverter stages powered via common resistor ⇒ on-chip common mode subtraction
- Common mode in noise distributions coupled in after inverter (via 2.5V)
- “Real“ CM appears on open channels that do not see the mean CM
- Edge channels are special: coupled to bias ring which is AC referenced to ground ⇒ strong noise if pre-amp reference (1.25V) fluctuates wrt ground ⇒ this is not subtracted
Common Mode & Differential Mode

Common Mode (CM)

- Signal source
- Noise source
- Stray capacitance
- Reference ground surface

Common Mode extraction: $I_{CM}$

DUT

Current Probe $\rightarrow$ Spectrumanalyzer

Differential Mode (DM)

- Signal source
- Noise source

Differential Mode extraction: $2I_{DM}$

DUT

Current Probe $\rightarrow$ Spectrumanalyzer
BCI: Mean Noise & Edge Strip Noise

On-chip CM subtraction is hiding real system response ⇒ concentrate on edge strips

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BCI: Cable Reflections

- Cable reflections can occur if cable length $L = n \cdot \lambda / 4$
  
  e.g. $f = 90\, \text{MHz} \implies \lambda = c / f = 2.2\, \text{m} = 2L$

- Peaks must move down if cable length is increased ✓

⇒ **Useful frequency range is below ~30\,\text{MHz}**

[Graph showing raw noise vs. frequency for different cable lengths]
BCI for Peak & Deconvolution Mode

Peak mode

APV Readout modes:
- **Peak**: 1 sample is used, $\tau = 50\text{nsec}$
- **Deconvolution**: weighted sum of 3 consecutive samples, $\tau = 25\text{nsec}$
**1-Step vs. 2-Step Conversion Scheme**

### 1-step scheme

- 1.2V chips
- FE-hybrid
- ~10V

### 2-step scheme

- 1.2V chips
- FE-hybrid
- ~2.5V
- ~10V

**Buck converter** plus **switched-capacitor converter ("charge pump")**

- **Pro:** 2-step scheme provides more flexibility and avoids high conversion ratio
- **Con:** Efficiencies multiply and system is more complex

**Implementation** as before, but:

- \( r = \frac{1}{4} \cdot \frac{1}{2} \)
- charge pump: chip, PCB, 3 copper layers, 2 x 1\( \mu \)F caps

⇒ Total TEC savings if both steps on hybrid: **7.0%** (cf. 1-step: 7.5%)
⇒ Total TEC savings for buck on petal rim: **7.0%** (cf. 1-step: 6.0%)