Status of MB4 Production

1. Dashboard
2. Updates
3. DDU

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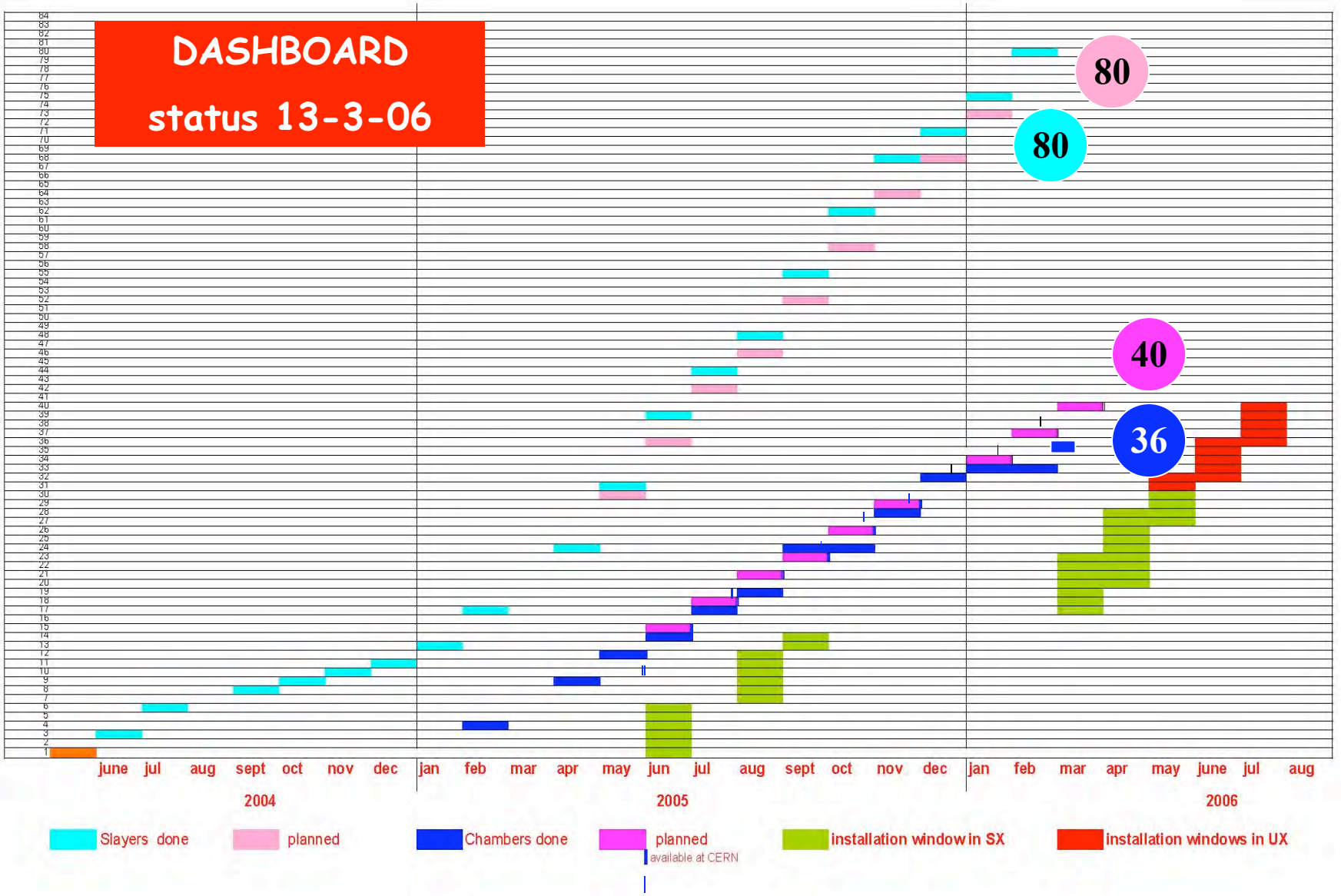
DASHBOARD
status 13-3-06
80
80
40
36
june jul aug sept oct nov dec jan feb mar apr may jun jul aug sept oct nov dec jan feb mar apr may june jul aug
2004
2005
2006
Slayers done
planned
Chambers done
planned
available at CERN
installation window in SX
installation windows in UX

Status of MB4 Production

SL Mechanically assembled	80 (80)
SL Tested	75 (80)
Chambers assembled	36 (40)
Chambers tested	33
Chambers at CERN	27

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Status of MB4 Production

- Production rate slightly slowed down due to contribution of people at CERN C&I
- SL: 2 chimney SL to do to complete nominal production. Chambers: 4 chambers to do.
- Expected to finish nominal production by mid april (standard chambers by end of march, chimney immediately afterwards). Chimney toolings ready, only mask for drilling corner blocks holes to be done. Common policy for the production line freezing?

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DT DDU/FED

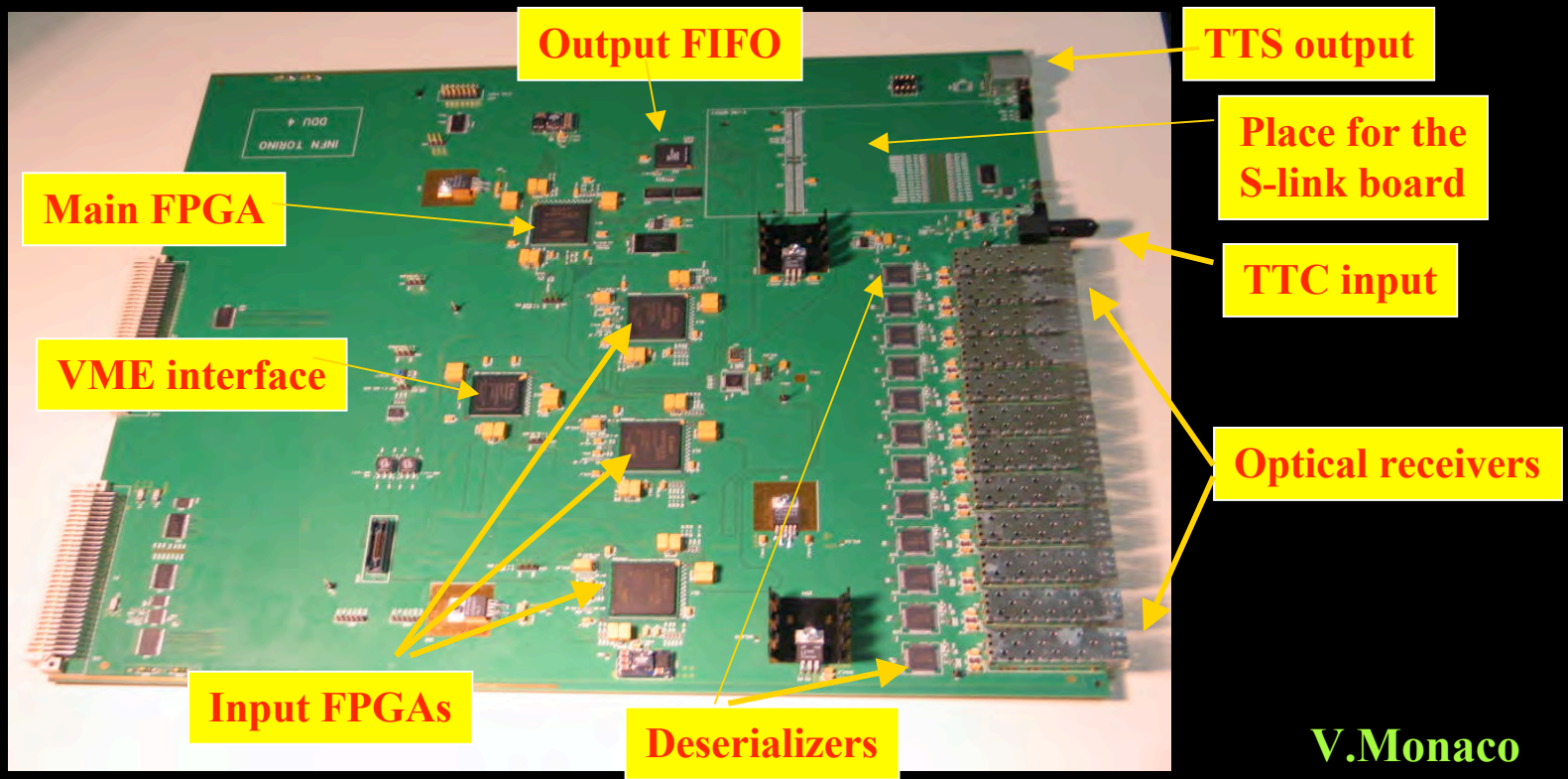
2 boards arrived. One board under test/debug:

Test and optimization of HW ongoing (few HW problems solved):

- Power ON (OK)
- VME interface (tested OK)
- clock distribution (tested OK jitter < 20 ps)
- FPGA loading (tested OK)

Working on:

- boundary scan software
- FPGA code debugging (data flow)
- TTC and TTS interface



V.Monaco

Status of DT DDU/FED

G.Dellacasa, V.Monaco
INFN-Torino

1 DDU pre-production board ready to be integrated in Legnaro, according to a schedule agreed two weeks ago.

- **Data flow from optical input to the S-link tested**
  - **ROS-DDU optical comunication OK**
  - **S-Link output tested with FEDkit and the FRL.**

- **A simulation showed a bad behaviour of the 64-bit internal bus when working at 80 Mhz. We lowered its frequency to 40 Mhz (the DDU band-width is still well above (320Mb/s) the maximum acceptable data rate of the FRL(200Mb/s)).**
  - no data corruption observe up to now at 40 Mhz

- **Merging of data from different channels under debug (could be ready in the next days).**

- **TTCrx still not working (we gave priority to prepare a board for the MTCC; the TTCrx problem will be debugged on another board after/during the integration tests in Legnaro).**

14/3/2006