



Bologna MC production



<http://www.bo.infn.it/~trava/DTminicrates.html>



DT Minicrates - Bologna Assembly Site



HOME DOCUMENTS TALKS STATISTICS PARTS PEOPLE PICS LINKS

Infos on MC already delivered

NEW! : Fotografie utili e interessanti nella sezione Pics !

NEW! : Frequently Asked Questions in italiano nella sezione Documents)

NEW! : Schedula aggiornata al 14 settembre

NEW! : Versione 4.12 del Test Boundary Scan (correzione di alcuni bugs)

(scarica versione .zip del codice per Windows Visual C++ 6.0 ; 1.8 Mbyte)

Docs on:
MC assembling and test
F.a.q.
(still in italian...)

Schedule on MC in progress





Bo MC prod - Status

Data from F.Dal Corso: see his talk for global consideration:
Here only Bologna rate will be discussed

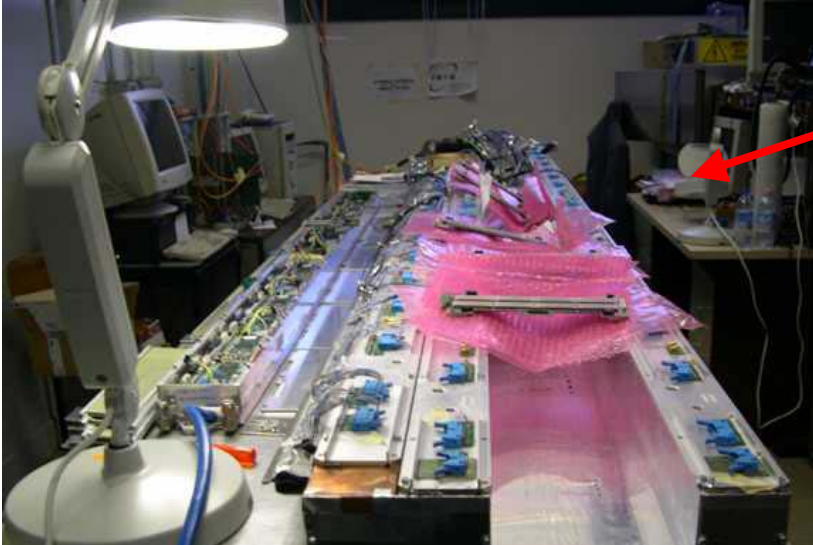
date	MC produced			
	LNL	Bo	MC/month	MC total
Sep-04	2		2	2
Oct-04	2		2	4
Nov-04	5		5	9
Dec-04	1		1	10
Jan-05	2	2	4	14
Feb-05	6	4	10	24
Mar-05	7	4	11	35
Apr-05	1	4	5	40
May-05	10	6	16	56
Jun-05	10	9	19	75
Jul-05	12	6	18	93
Aug-05	3	5	8	101
Sep-05		6	6	107
	61	46	107	

↓ Training phase
↓ Ununderstood TRB timing problems

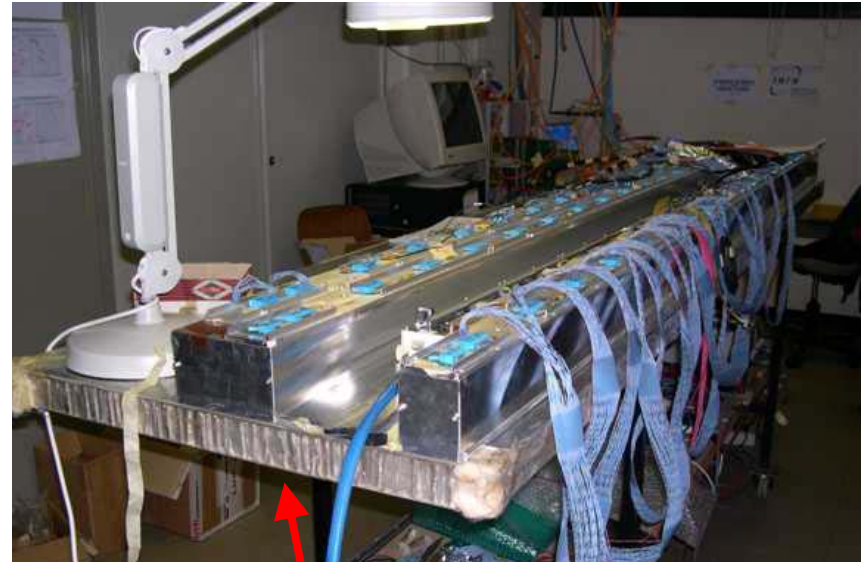
→ 1 stopped week: Problems on test setup
→ 1 holiday week
→ Data at 19/09/2005

Status (BO): 46 MC delivered up today – Actually rate \cong 2 MC/week

Bo MC prod - reminder



Step 1: assembly and boundary scan



Step 2: full test of Minicrate



Step 3: dressing



Bo MC prod – status (2)

Actually:

- 2 MC are assembled and tested in parallel (one station for full test)
- final dressing is done on a chamber FE mock-up having all connectors, although NOT equipped with FE boards.



Ideal rate: 2.5 MC/week

But...

Board changing rate \approx **1.2 board/Mc**

(N.B. Board changing rate is NOT board failure rate!)

\Rightarrow Tests must be repeated starting from the Boundary Scan;

\Rightarrow Effective rate : \approx **2 MC/week**

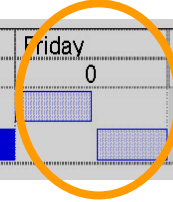


Bo MC prod -future



Assembly and Boundary Scan Test done by external firm

ID	Task Name	Duration	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
1	Trigger assembly	4.5 days	0	█	█	█	█	█	0
7	Boundary Scan Test	4.5 days	0	█	█	█	█	█	0



Test-Stand Occupancy

contingency

ID	Task Name	Duration	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
1	Dynamic Test	0.5 days	0	█	0	0	0	0	0
2	FE cabling + full test	1 day	0	█	0	0	0	0	0
3	Dynamic Test	0.5 days	0	0	█	0	0	0	0
4	FE cabling + full test	1 day	0	0	█	0	0	0	0
5	Dynamic Test	0.5 days	0	0	0	█	0	0	0
6	FE cabling + full tes	1 day	0	0	0	█	0	0	0
7	Dynamic Test	0.5 days	0	0	0	0	█	0	0
8	FE cabling + full test	1 day	0	0	0	0	█	0	0

Test-Stand Occupancy will be the limiting factor!

Dressing on a chamber FE mock-up

ID	Task Name	Duration	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
1	Dress	0.5 days	0	0	█	0	0	0	0
2	Dress	0.5 days	0	0	0	█	0	0	0
3	Dress	0.5 days	0	0	0	0	█	0	0

=> 3 MC/week seems an achievable rate



Bo MC prod – future (2)

Assembly & BSC test by external firm

Terms

- Tender on going ; works should start at beginning of Oct.
- Partially flexible contract: interruption periods can be foreseen;
Min: 1 month (20 MCs) – Max: 5 months (100 MCs)

Requirements

- Reduced test system (PC, power supplies, TTC clock) : procurement on going
 - Adequate buffer of available parts (everything but signal and test pulse cables) :
 - MC (+ parts from Ciemat) buffer in Legnaro \approx 50 (foreseen at beg. Of Oct.)
 - Boards production:
 - TRB : we need \approx 120 per week
 - CCB : we need \approx 20 per week with new array resistors
- This week we check Board availability and production rate with F.Dal Corso

We could plan to start beginning of Oct. till half December (\sim 50 MC) @ 4÷5 MC/week



Bo MC prod – summary

- ✓46 MC produced up to now
- ✓2 MC/week (8 MC/months) is the actual production rate in Bologna (good but still critical in case of any kind of problem)
- ✓A 50% boost is expected from Oct. when the assembly and BSC test will be performed by an external firm.
(Parts availability has to be carefully verified and guaranteed)

Infos:

- New Web page for MC production in Bologna
- Boundary Scan Test – Manual is in preparation