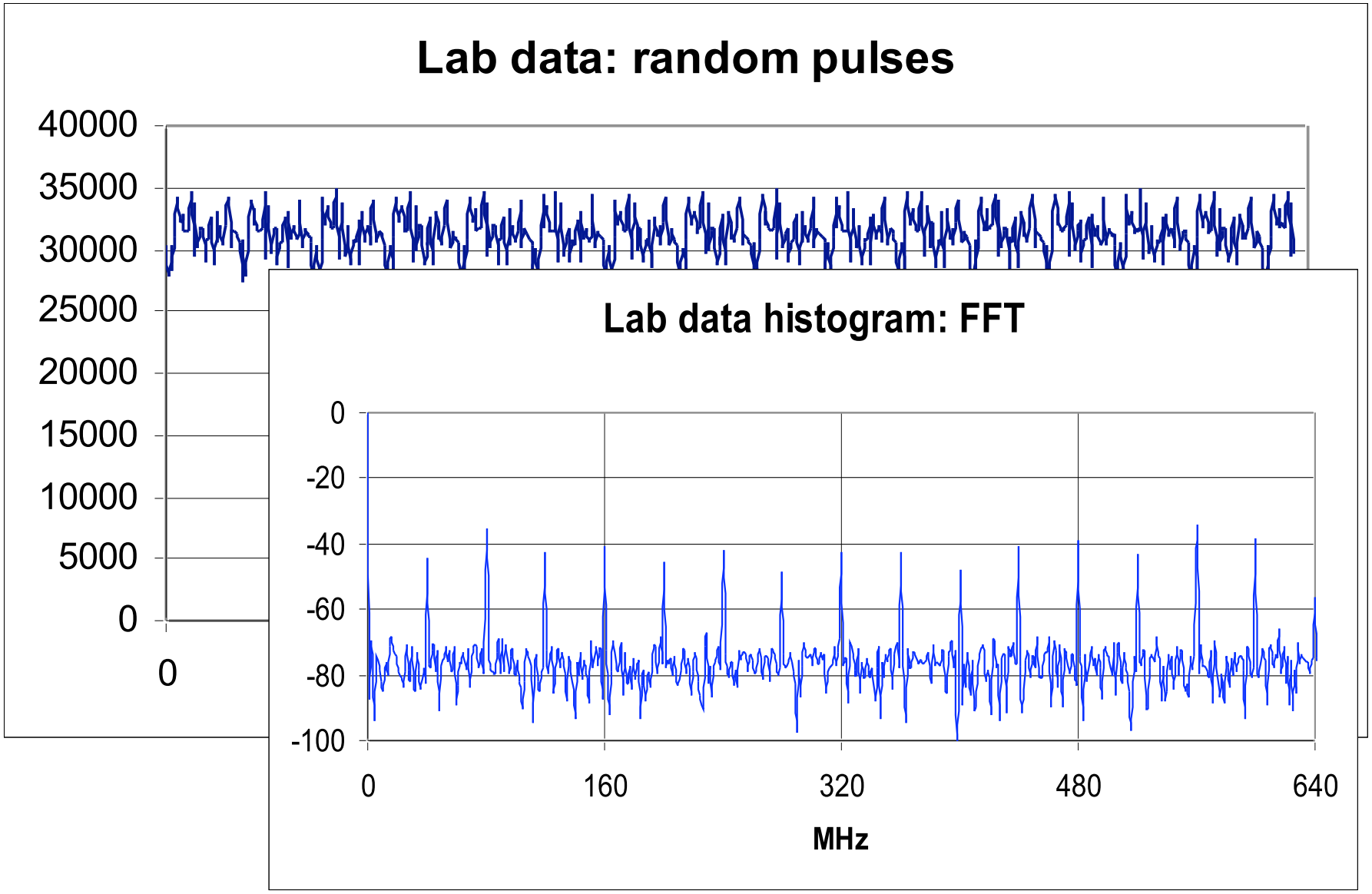
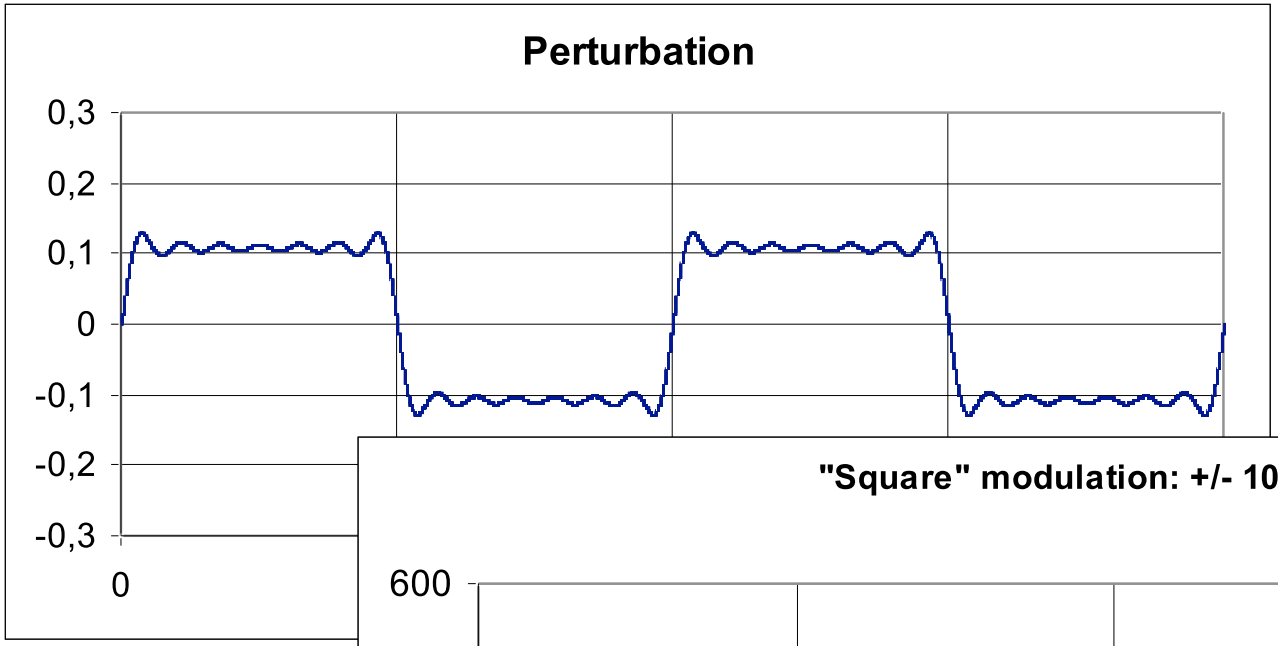
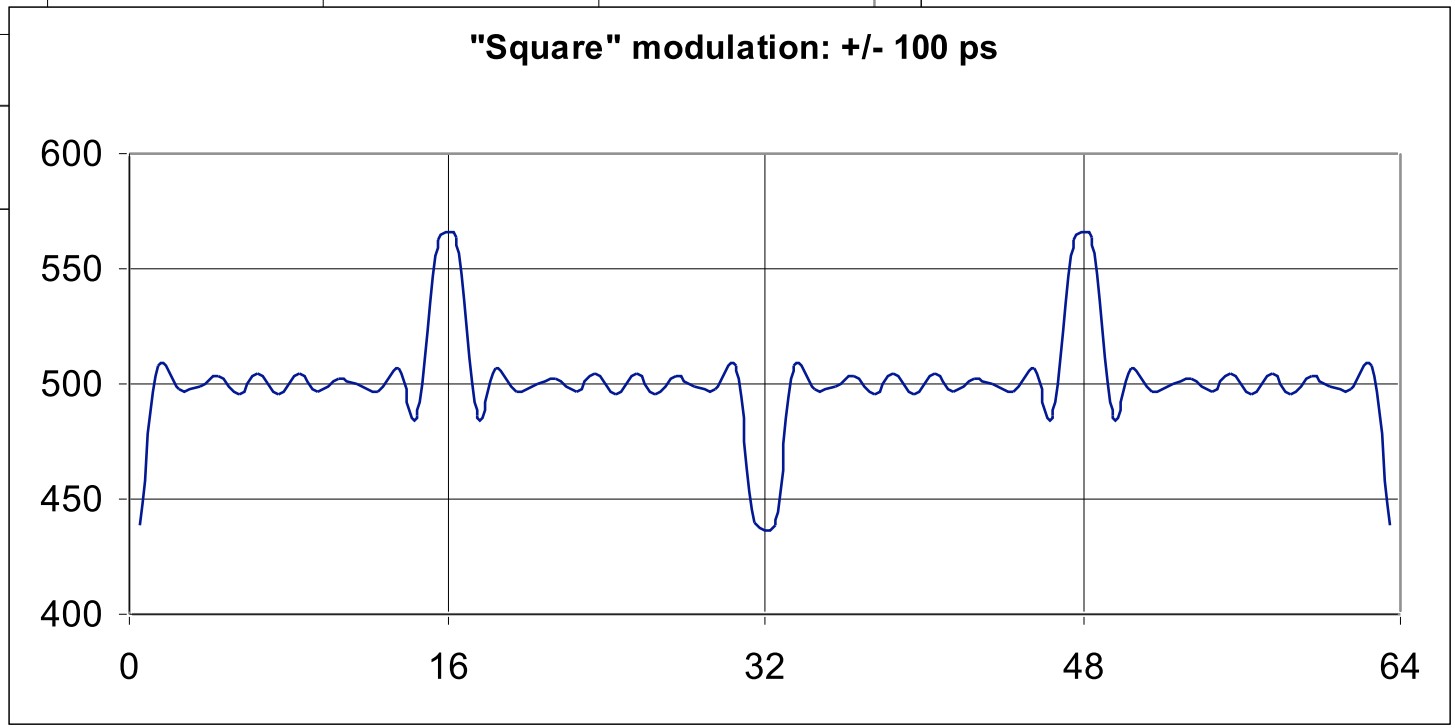
40 MHz patterns

40 MHz patterns

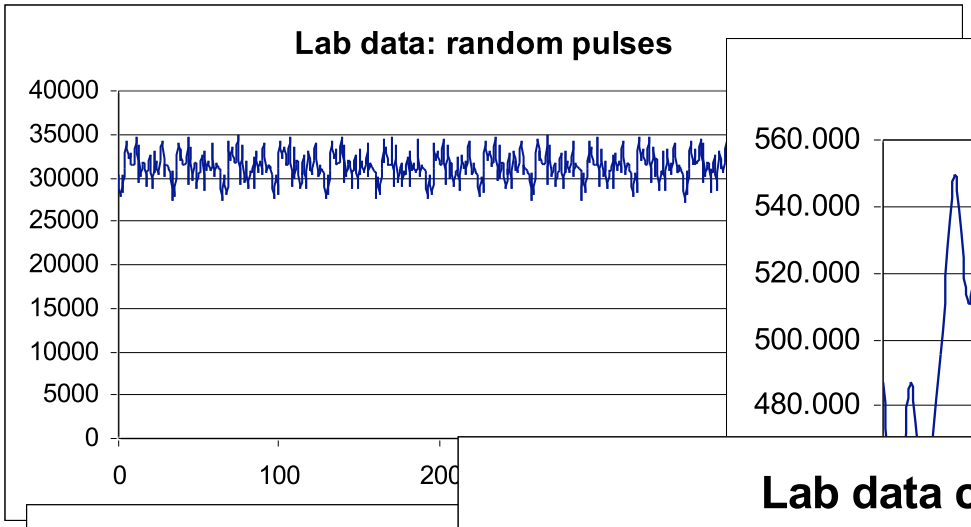


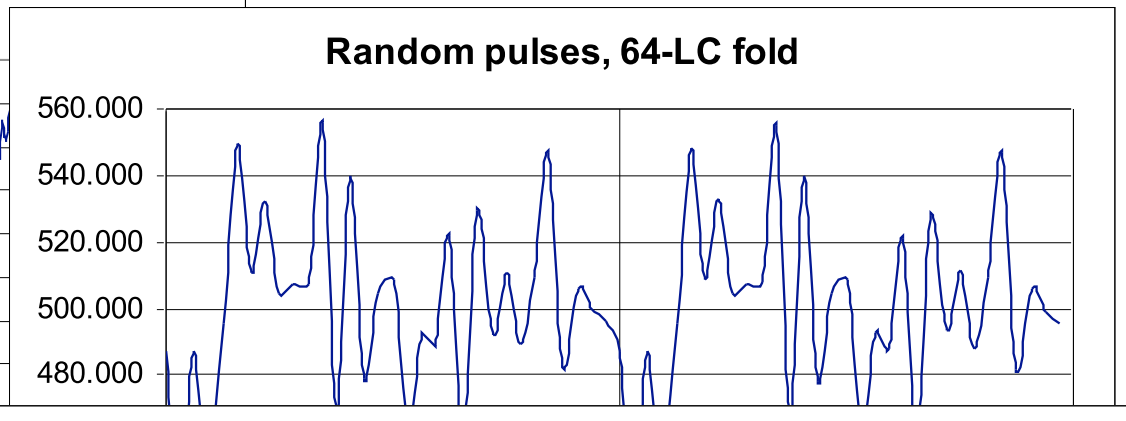
Simulation

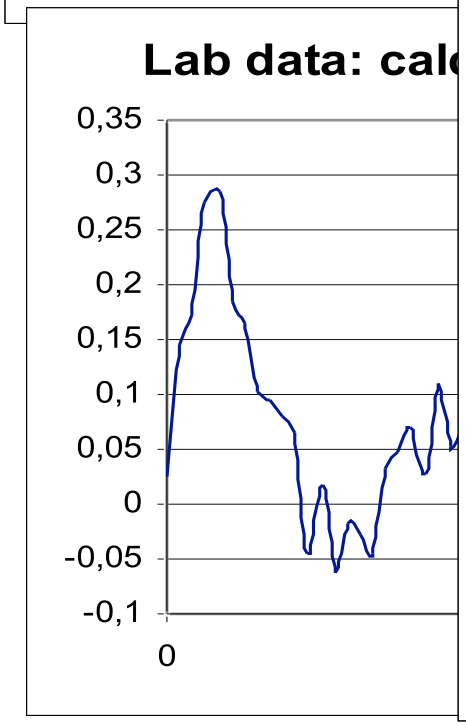

Perturbation
0,3
0,2
0,1
0
-0,1
-0,2
-0,3
0

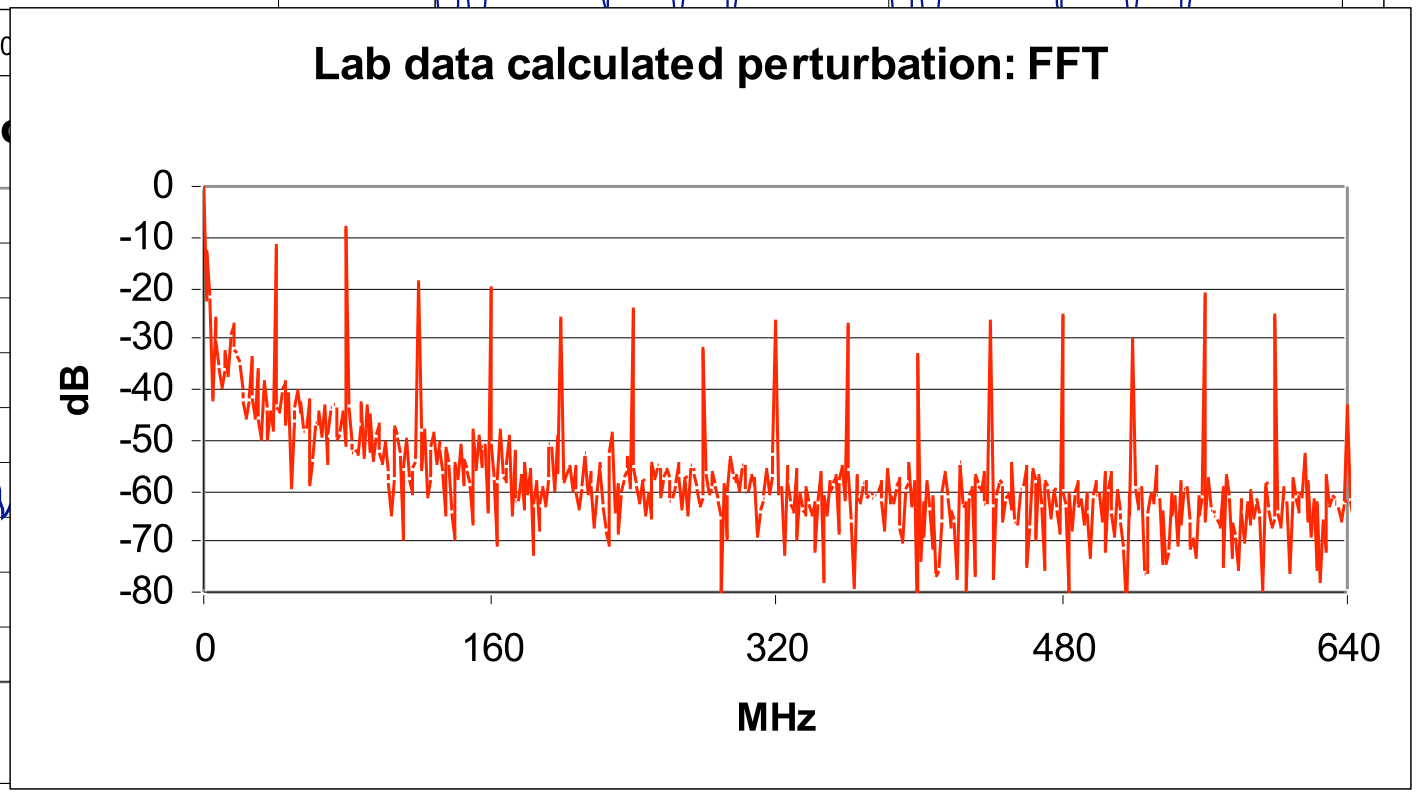

"Square" modulation: +/- 100 ps
600
550
500
450
400
0
16
32
48
64

Pattern Analysis

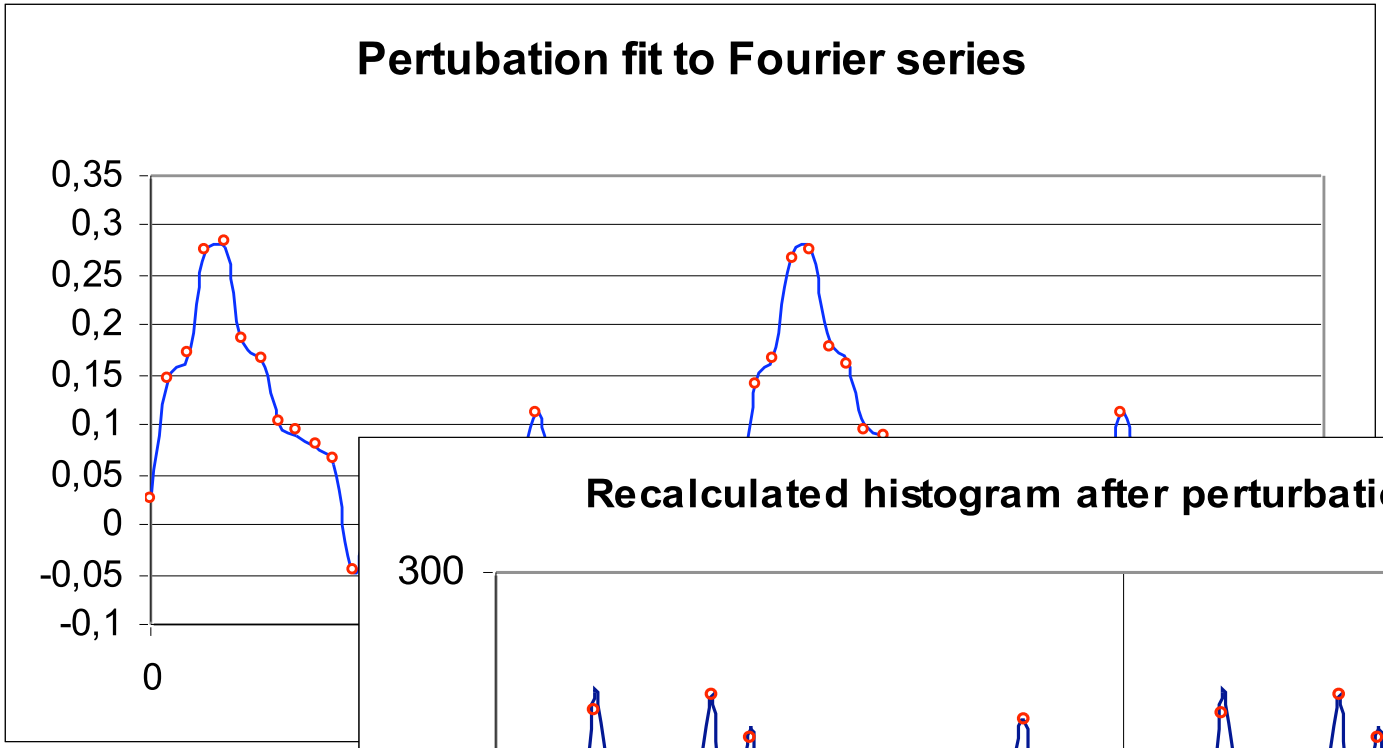


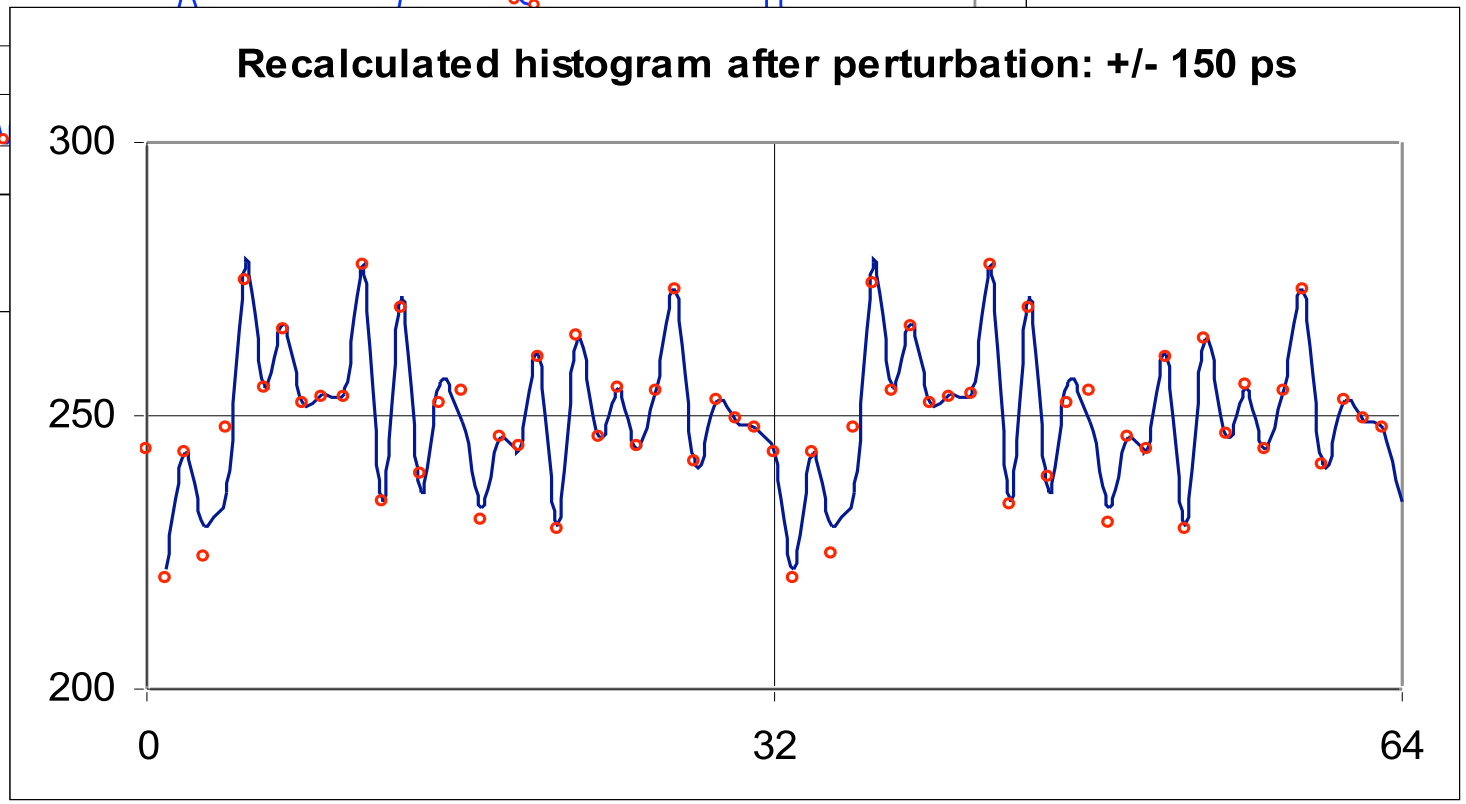






Analytical Pattern Reconstruction





TDC Specifications

27. Technical Specifications.

Number of channels:	32 / 8	
Clock frequency:	40 MHz external 40MHz / 160 MHz / 320 MHz internal	
Time bin size:	781 ps	low resolution mode
	195 ps	medium resolution mode
	98ps	high resolution mode
	24 ps	very high resolution mode (8 channels)
Differential non linearity:	Typical values	
	+/- 0.2 bin	0.08 bin RMS low resolution mode
	+/- 0.3 bin	0.09 bin RMS medium resolution mode
	+ 0.60, -0.25 bin	0.10 bin RMS high resolution mode
	+0.35, -0.25 bin	0.08 bin RMS high resolution mode (DLL corr.)
	+1.3, -0.7 bin	0.21 bin RMS very high resolution mode
Integral non linearity:	Typical values	
	+/- 0.25 bin	0.11 bin RMS low resolution mode
	+/- 0.50 bin	0.24 bin RMS medium resolution mode
	+0.6,-1.4 bin	0.50 bin RMS high resolution mode
	+3.5,-5.0 bin	2.1 bin RMS very high resolution mode

TDC DNL and INL

28. Time resolution measurements

The time resolution of the HPTDC 1.2 have been measured with different schemes to characterize the effective performance.

Differential and Integral non-linearities have been measured with code density tests using a random source of hits. Code density tests are very efficient to measure DNL and INL but must not be taken as a measure of the effective time resolution of a TDC device as all error components of random nature (e.g. jitter) are excluded from the results. Code density tests are also very useful to optimize the RC-delay chain and DLL tap adjustments.Non-linearities are only shown covering a time period of 25ns as the TDC architecture, using a simple counter to extend the dynamic range, insures that the patterns shown are repeated identically for each 25ns period

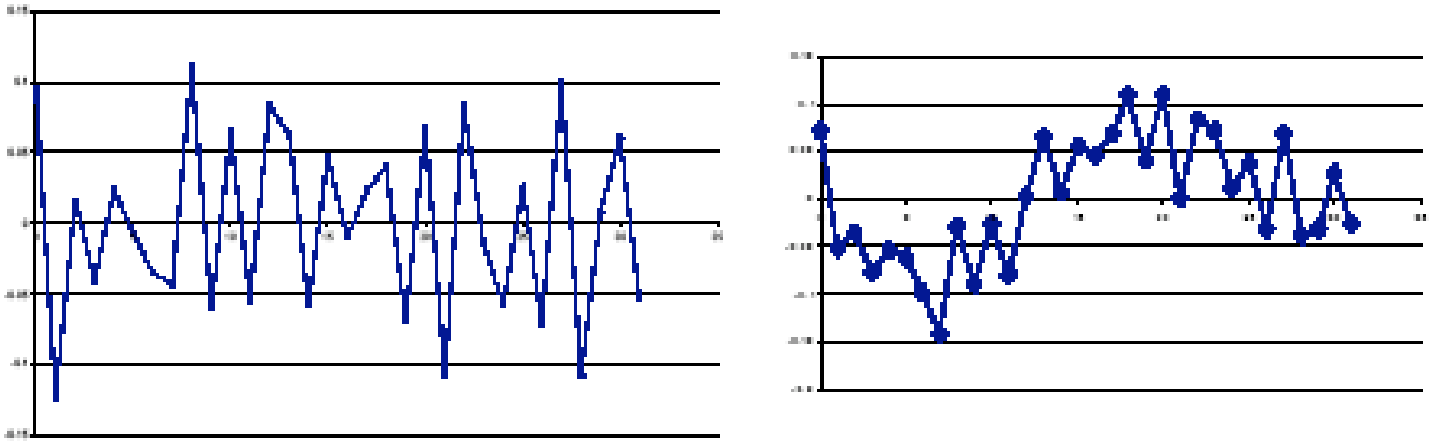
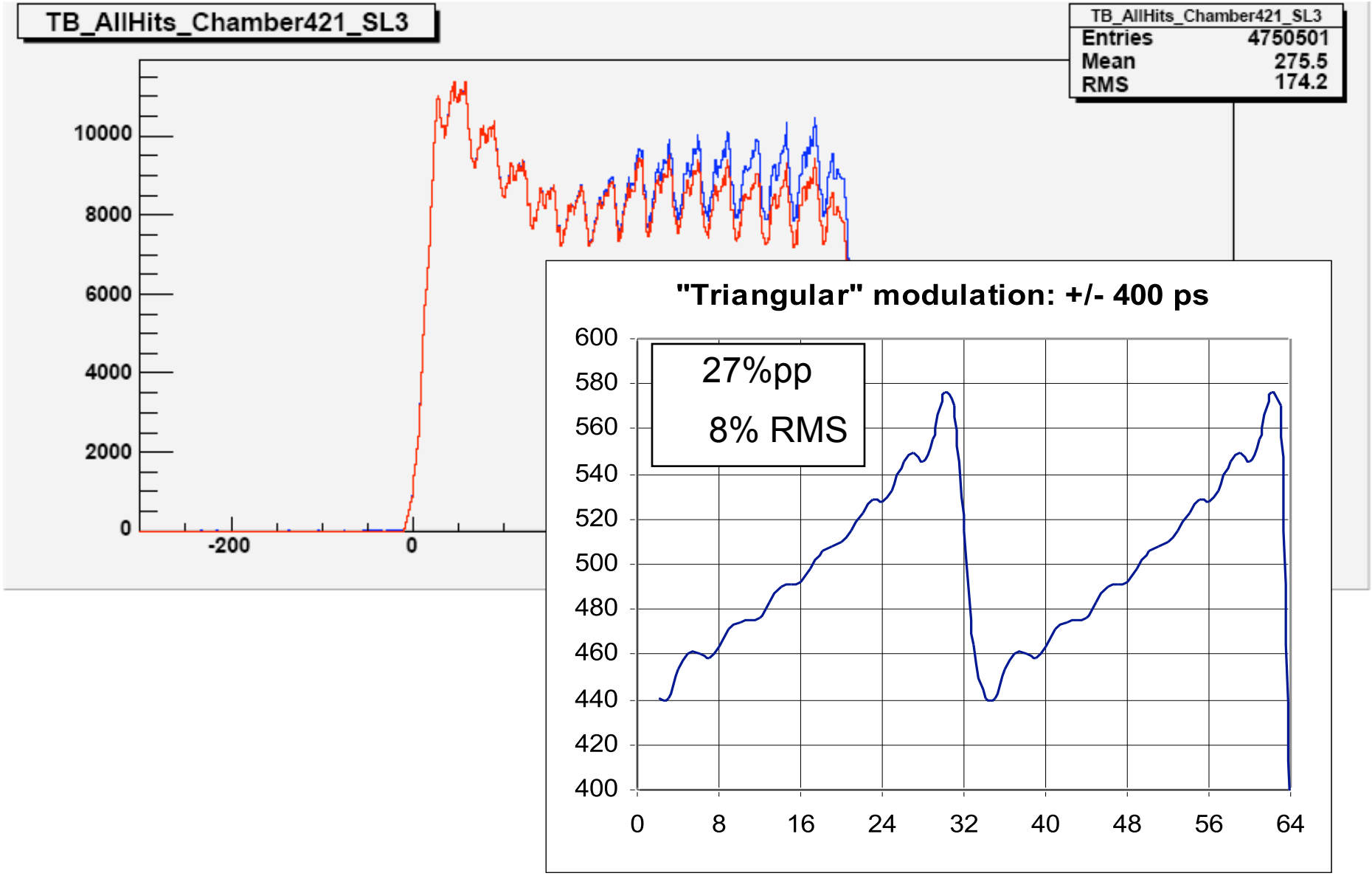


Fig. 33 DNL and INL in low resolution mode

Nasty Histograms



Mathematics

Some mathematical relationships

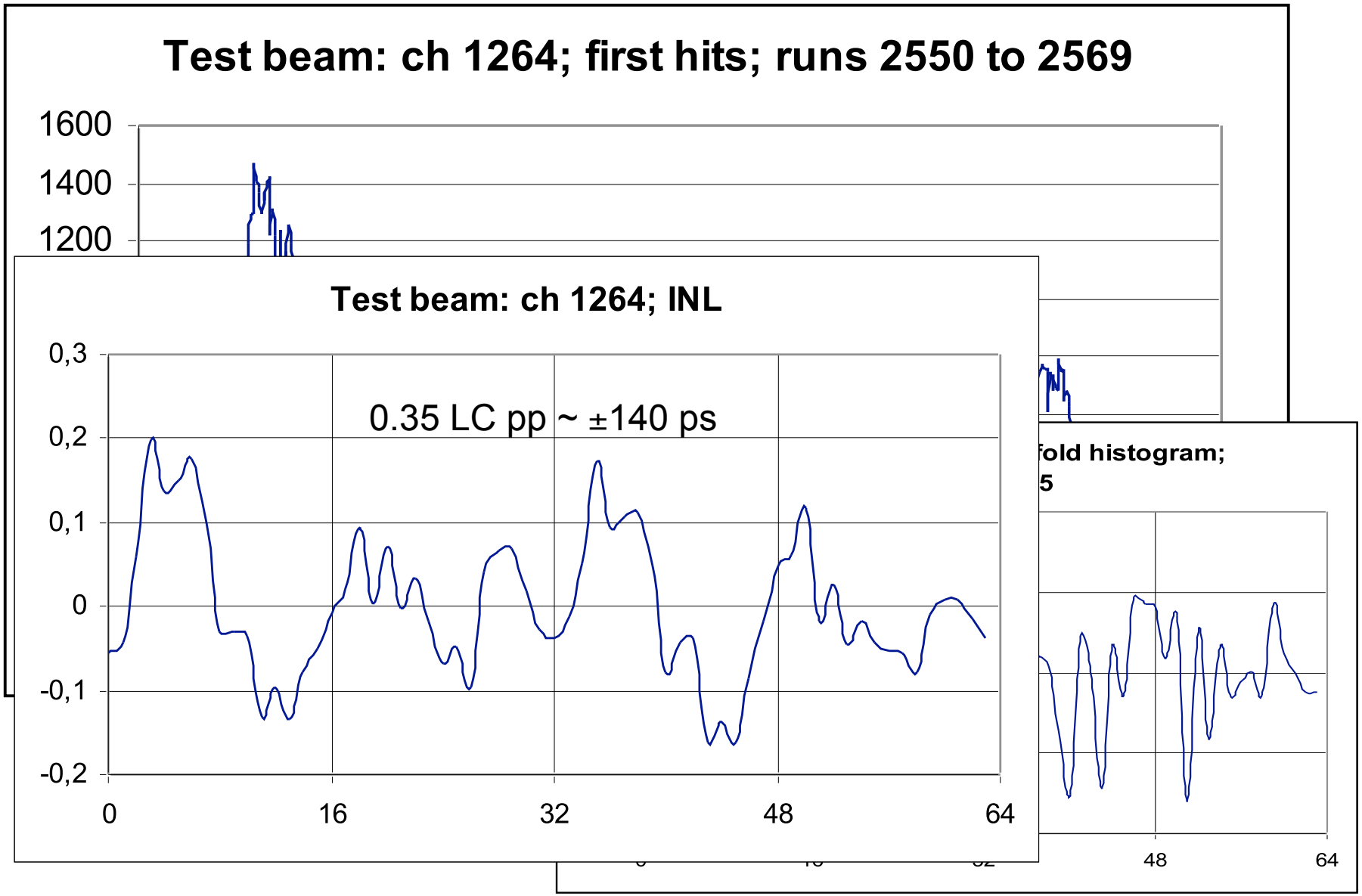
- Time-box histograms are a kind of "code density plots" which are directly related to differential non linearity (DNL).
- But we are interested in integral non linearity (INL) which can be calculated from DNL plot by integration.

Receipt

- Calculate DNL: dnl(i) = h(i)/histogram_mean_value – 1
- Calculate INL : inl(i) = inl(i-1)+dnl(i)
- Find MAX, MIN in INL. These are maximum time deviation in TDC LC's.

Hints: to have meaningful results statistics fluctuations must be negligible. In practice counts per bin should be 10000 counts or higher. Use a flat region of the time-box.

Example


Test beam: ch 1264; first hits; runs 2550 to 2569
1600
1400
1200
Test beam: ch 1264; INL
0.35 LC pp ~ ±140 ps
0,3
0,2
0,1
0
-0,1
-0,2
0
16
32
48
64
old histogram;
5
48
64

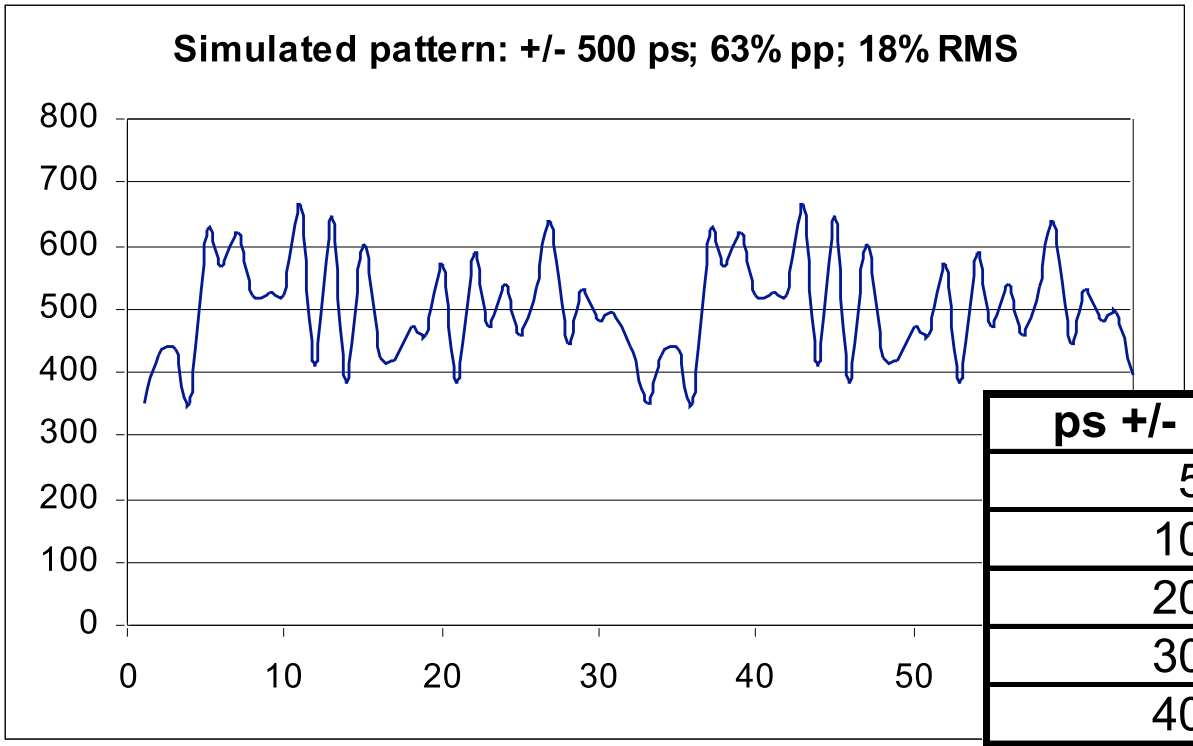
Conclusions

- This effect can be explained as a phase modulation by clock harmonics.
- Small arrival time shifts may cause large visual effects in drift time histograms.
- Worst case configurations we manage to setup in our Lab seem to correspond to arrival time variations in the range of 100-200 ps, compatible with TDC specifications (INL).
- Most likely there is not a single source of phase modulation, but a sum of small effects across the whole system.

Next steps

- Isolate and quantify possible sources: TDC, ROB, TRB, cabling, PS, grounding ...
- Study multiple pulses case.

Simulated patterns



ps +/-	pp %	RMS %
50	7,4	1,8
100	14,8	3,7
200	29,6	7,5
300	42,6	11,2
400	52,7	14,7
500	63,1	17,8
600	73,0	20,7
700	85,0	24,2
800	106,8	28,0
900	120,5	30,9
1000	128,8	33,1