HV Supply Commissioning

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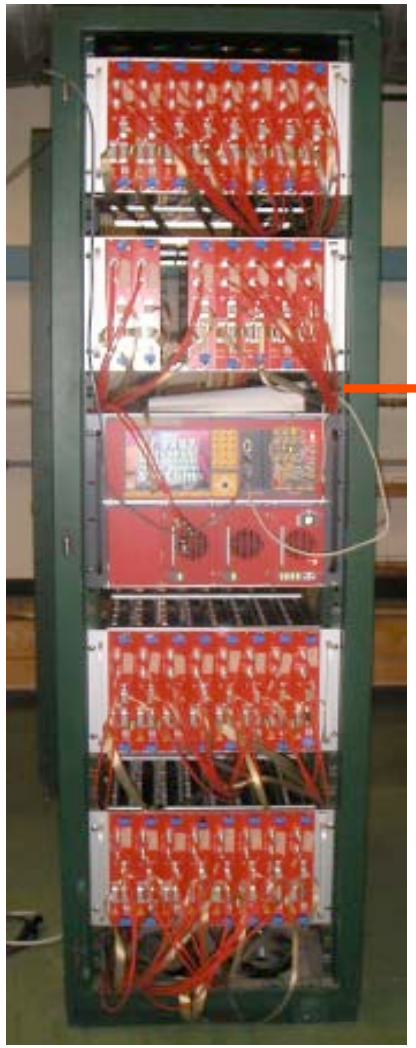
MU DT Chambers Meeting

CMS WEEK 20th September 2005

Hardware Test Unit



8 A876 boards

32 A877 boards

corresponds to
1/8 of the whole system

Tests planned

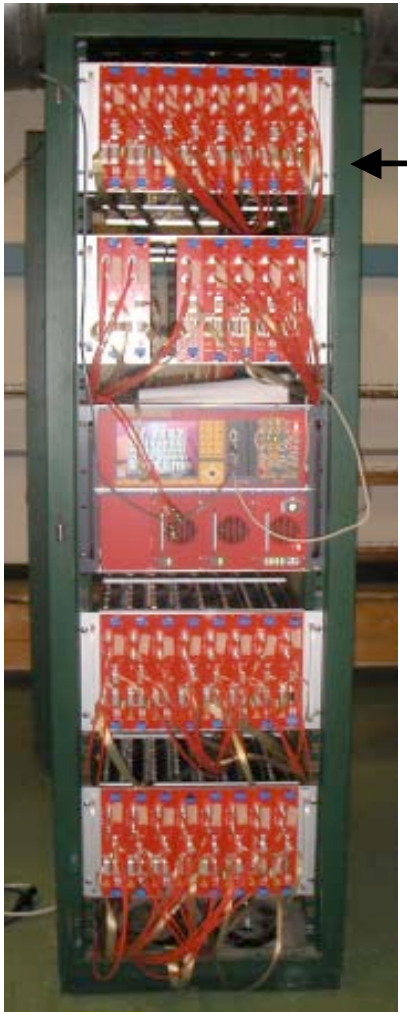
- 6 different tests:
  - Test 1: Min. voltage, Max. current (test A877 partitioning transistors)
    - use resistive loads (10 M Wires and Strips, 3.9 M Cathodes)
    - 4 days per board
  - Test 2: Max. voltage, Max. current (test A876 generator)
    - use resistive loads (300 M Wires, 160 M Strips, 60 M Cathodes)
    - 1 day per board
  - Test 3: Ramping cycles (test A877 transistors in variable conditions)
    - use RC loads
    - 1 day per board
  - Test 4: Min. voltage, Null current (test electronics of both modules)
    - No load
    - 7 days per board
  - Test 5: Test at nominal voltage
    - use RC loads
    - 2 day per board
  - Test 6: Independent (direct) measurement of the voltages
    - use voltage dividers (values read using a multimeter)

Hardware & software

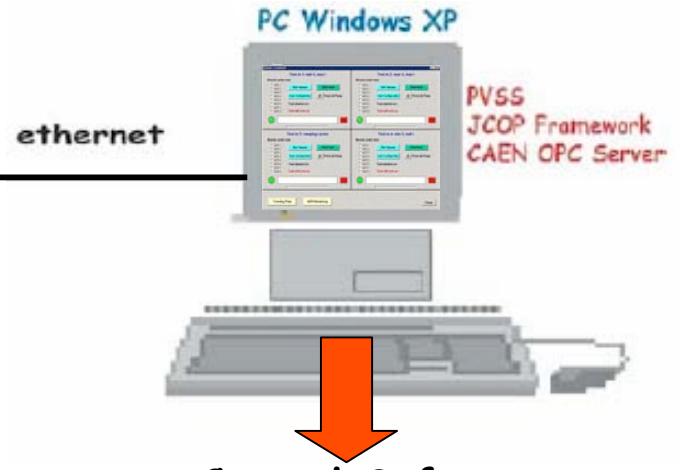
- Hardware requirements:
  - Rack
  - A876↔A877 cables (64 HV, 32 LV, 8 Communication)
  - Dedicated PC
  - Loads
    - 24 units for Test 1 (8 boards tested simultaneously)
    - 24 units for Test 2,3 and 5 (8 boards tested simultaneously)
    - 1 unit for Test 6
- Software requirements:
  - Control software (PVSS dedicated program)

Done: test set up at the ISR

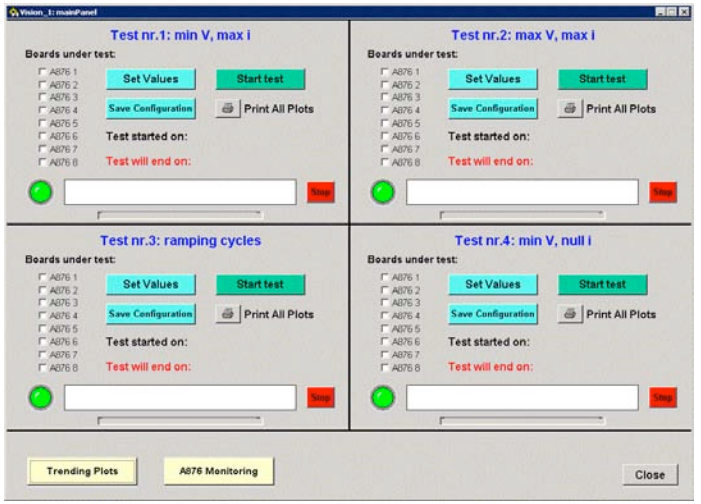
Rack & cables



PC



Control Software



Done: Test 4

- Done first because it does not require loads
- Performed between April 25th and June 13th
  - 32 A876 boards tested
    - no problems found
  - 166 A877 boards tested
    - 9 sent back to CAEN to be repaired
- Summary HV boards: tested + used for chambers at ISR
  - 5 SY1527 power supplies
    - 2 problems
  - 40 A876 boards
    - no problems found
  - 185 A877 boards
    - 15 problems

Summary of the problems

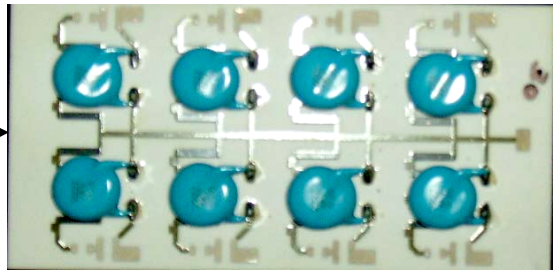
- SY1527 power supply:
  - 2 communication problems
    - CPU substituted

- A877 boards:
  - 2 Calibration Errors
    - need to be calibrated again
  - 5 OvC, discharges, noises…..
    - (mechanically) broken capacity or resistor, cabling error
  - 5 UnV
    - (mechanically) broken capacity or resistor
  - 3 OvV
    - broken voltage divider

➲ All the problems promptly solved by CAEN

Future Schedule

- Load Units:
  - first prototype built and tested by E. Borsato
  - required material delivered
  - construction will soon start in Bologna



(RC prototype)

- Estimated time for tests:
  - Due to the available number of load units:
    - 2 weeks minimum for each set of boards

→ 4 months for the whole detector

Conclusions

- All the required material has been delivered; we are waiting for the assembly of the load units
- 1/8 of the system is tested simultaneously (2 weeks)
- 4 months needed to test the whole system