DT Session, CMS Week 040920-24

Status of HVB and PADC production

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Summary of status:

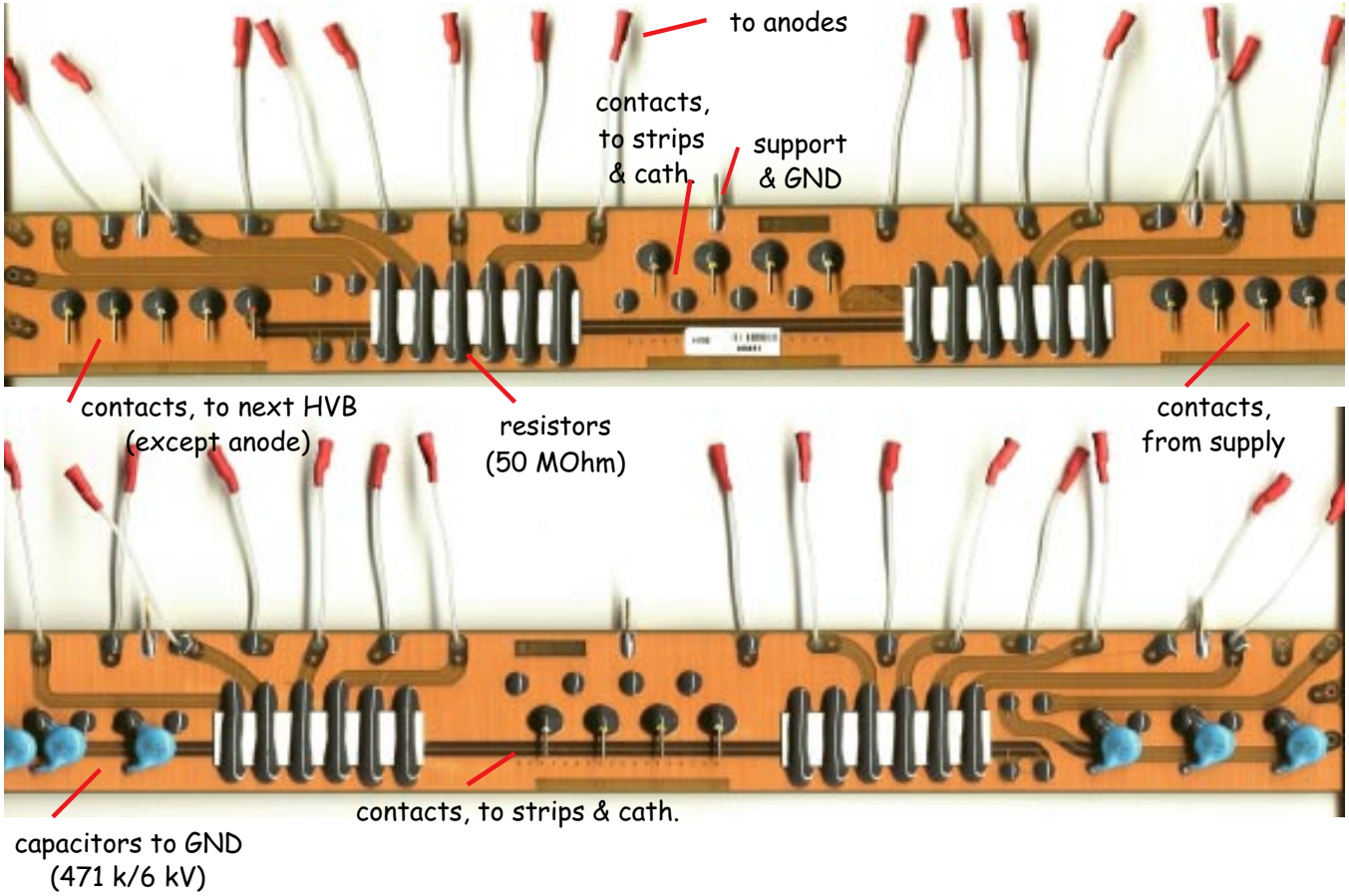
HVB_v5:

- HV pins protected, now
- All tests passed (small samples; risk estimated low)
- ~1750 PCBs received, ~60 assembled
- Urgent order of further batches (keep multiple vendor)
- Mech. update of new test jig to be done.
- Substitution in chambers is critical work (time, schedule).

PADC:

- All assembled; calibration & QC o.k.
- 50 units shipped; further 50 arrive next week (of 250 total).

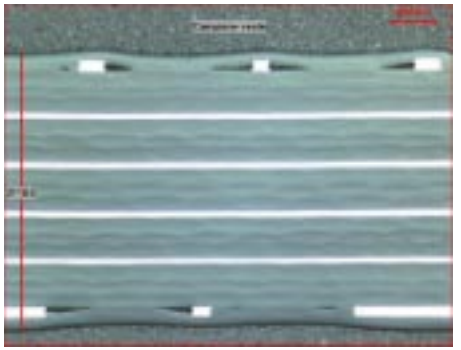
HVB: Function & Weakness



Top and bottom view of an HVB_v1.
It is a HV distribution board for up to 20 drift cells:
- 6 independent voltage channels from the supply (2 for anodes, strips and cathodes) ; strip and cathode voltages are passed to the next HVB for coarser granularity.
- 24 resistors (1 per anode and 1 per 10 strips and 10 cathodes).
- 6 capacitors (1 per HV channel)
- daisy-chain cables to strips and cathodes (not shown)
- 6-layer PCB; path for each voltage channel in one layer; innermost layers for cathodes, outer layers for anodes.

Main weaknesses:

- Small track distances of **0.45 mm/kV**
- Gas inclusions on outer layers (under prepreg "no flow")
- Unprotected HV pins.



Section of HVB_v2:

Cu layers (6) are white,

dark spots next to Cu are gas inclusions.

HVB Failure

It has been realized that:

- HVBs passing QC tests could still fail
- Even after long time running (~3000 h) failures appear - too many for use at LHC

In February 2004 then decided to:

- Develop a substitute HVB, maintaining external geometry
- Produce full batch of HVB substitutes (~11000 16-/20-channel and ~350 8-channel HVBs)
- For interim installation use some HVB_v2 (have somewhat increased distances in outer layers)

Note:

- HVB_v2 also have gas pockets and are prone to failure.

New HVB: HVB_v5

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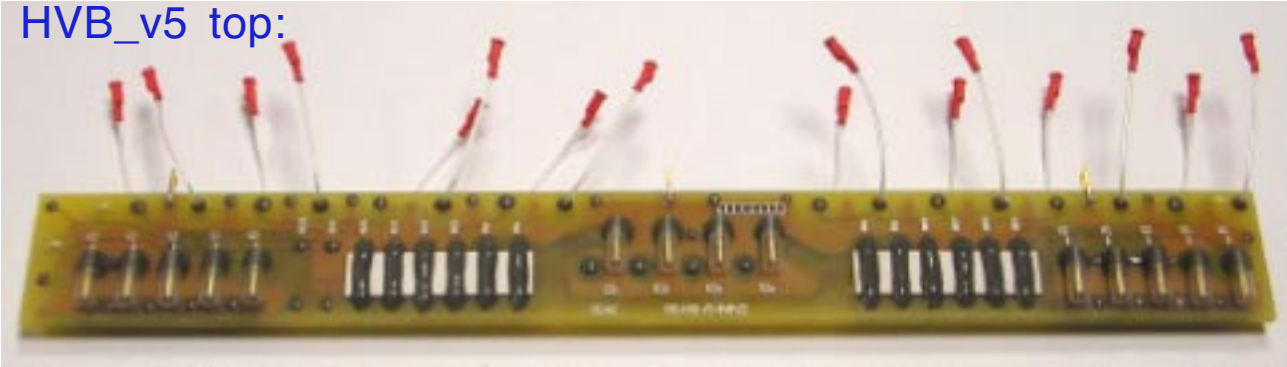
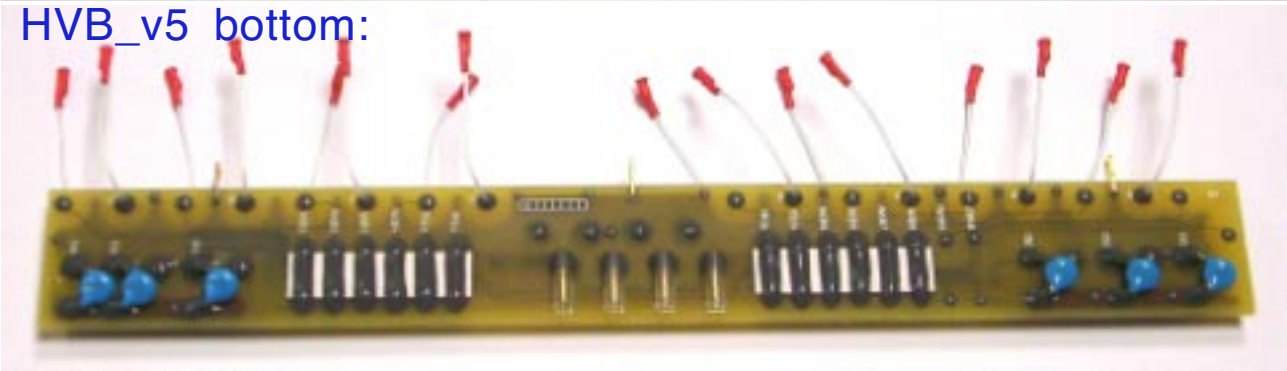
HVB_v5 top:

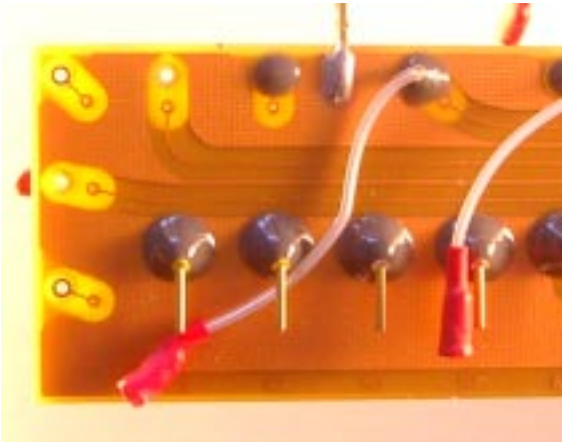


HVB_v5 bottom:



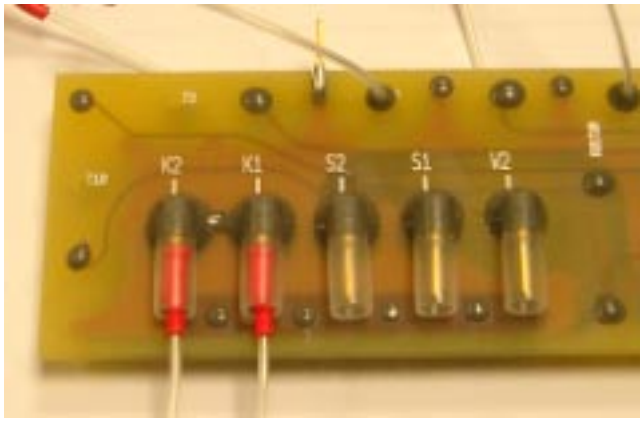
HVB_v5 main features:

- No “no flow” prepreg
- Distances **>1.5 mm/kV** everywhere
- No naked HV pin
- 8 layers



HVB_v1:

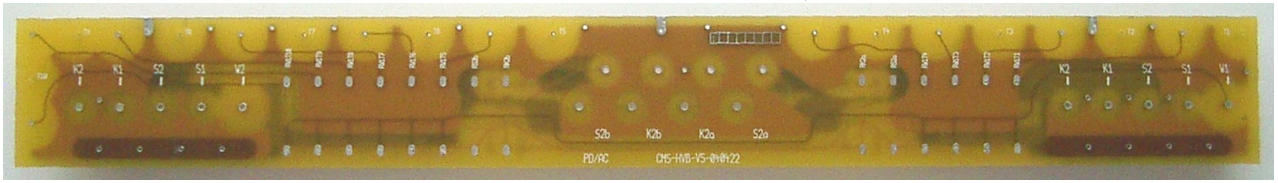
Unprotected HV pins



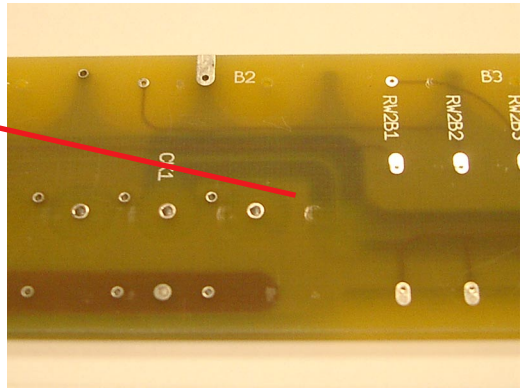
HVB_v5:

HV pins have **protection**. Will use **dummy plug** where no female plugged

HVB_v5 Production, Validation

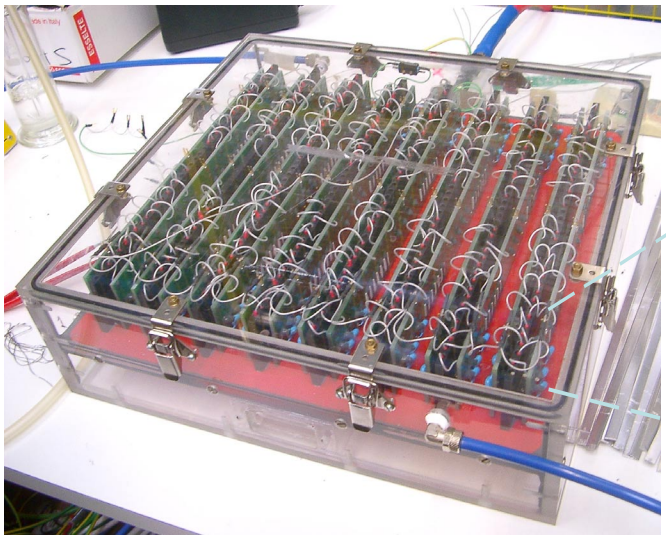


- Layouts finished - both for 16-/20- and for 8-channel versions.
- Ordered first samples/batches from *three* firms: 25+2000, 200+350, 2000, respectively. The 350 are all 8-channel HVBs needed.
- Received from one firm 25 in June, then 200 in July, then 1331 last week. From the other firm received 200 in July.
- Ordered first sample/batch of pin protections and of plugs. 10k pin protections and all plugs needed during assembly shipping this week. Received preseries of pin protection.
- Assembled 30 HVBs at Aachen, 20 at Legnaro, 20 at IHEP.
- Ordered pin protection 10k and plugs; mounted preseries sample on two HVBs.
- 200 HVBs, shipped to IHEP now, were thermally cycled. Advantage of cycling being questioned; considering to discontinue.
- Tested in air, in jig with gas and in chambers (next slides).
- Protruding tin from one PCB occasionally marks neighbour.
- Therefore next PCBs without tin.
- IHEP preparing to assemble ~1200-1400 monthly.
- Retrofitting HVB_v5 into chambers is a major action!

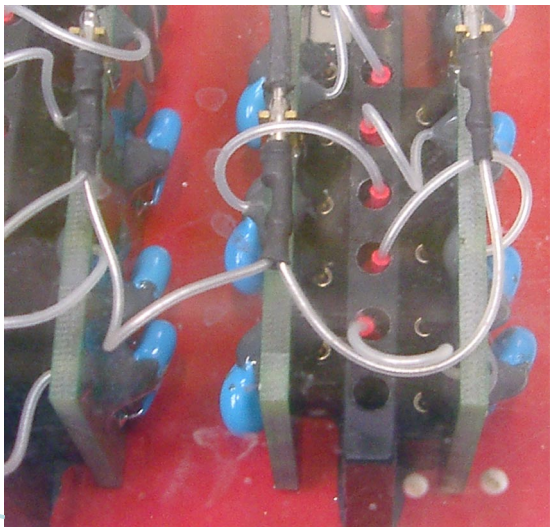


HVB_v5 Tests at Legnaro

- Tested ~20 *freshly* assembled HVBs in Ar/CO2 gas at +5/+2.5/-2.5 kV (at anodes/strips/cathodes), i.e. at overvoltages (w.r.t. nominal +3.6/+1.8/-1.2 kV) and saw some sporadic small current of ~100 nA. Same also observed at IHEP, on ~20 tested.
- Test jig and voltages are as used for mass assembly.
- Tested 18 in 1 SL (Legnaro) for about 2 month at normal operation; all fine.
- When the same test was repeated at Legnaro after HVB usage in chamber there was no current, fine. (It is what one could expect from humidity when fresh FR4 is not dried.).
- Tested 3 HVBs from Aachen (assembled at Aachen with PCBs from other firm) and found no current as well.



Test jig for 16 assembled HVBs under gas, available at Legnaro and at IHEP.



Detail of the test jig, showing HVBs supported via their pins and “parked” output connectors (red).

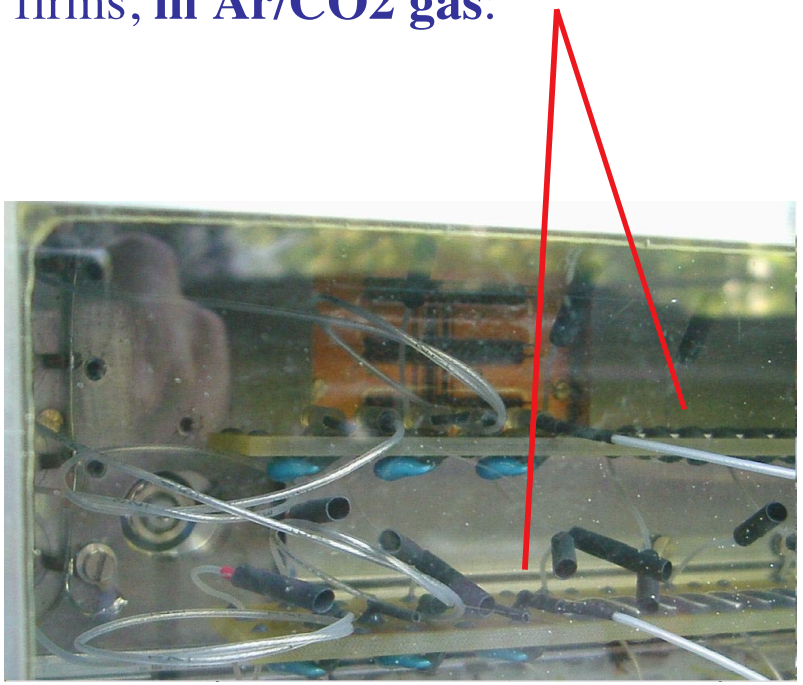
HVB_v5 Tests at Aachen

- Tested a few in air in June/July up to +6/+1 to +6/-4 kV (at anodes/strips/cathodes), in air for several days; no current *(means < 10 nA)*.
- Tested 24 in 3 SLs for about 2 month; all fine.
- Last week received 5 PCBs from Legnaro, from other firm. Assembled at Aachen.
- Tested 3 from Legnaro in air, voltages as above; no current.
- Test series on HVBs assembled with PCBs from 2 firms, **in Ar/CO2 gas**:

1. At +5/+2.5/-2.5 kV, 5 days; no current.
2. Raise to +5/+2.5/-**4** kV; no current until -3.5 kV for both, up to end of range for HVB with pin protection.
3. Raise to +**5.8**/+2.5/-2.5 kV; no current.
4. Raise to +**5.9**/+2.5/-**3.4** kV; no current.
5. Raise to +5/+**3.9**/-2.5 kV; no current.

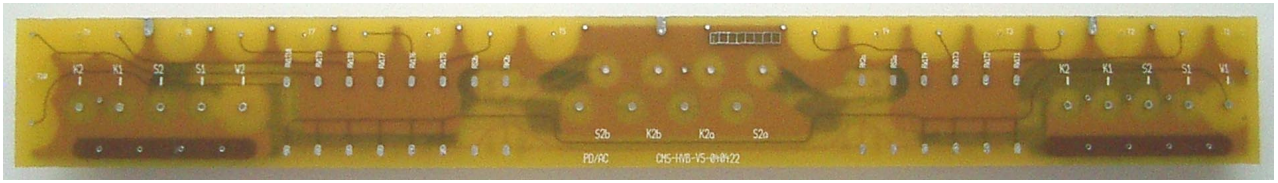
Note: raised from +5/+2.5/-2.5 kV in ~14-32 steps, lasting at each ~4 min.

Observed single discharges on *surface* of HVB without pin protection, before end of ranges above.



Two PCBs from two different firms, assembled at Aachen and being tested under gas. Top one has pin protections. Output cables have connector protected by insulating tube (black).

Further Orders, Assembly, Retrofitting



Next actions:

- Update test jigs' mechanics for compatibility with pin protections - small but URGENT -
- Place next orders for PCBs. Without tin? (One of the firms wants to keep tin.)
- Continue testing some boards at Legnaro and Aachen; especially sample from large batches. E.g. Aachen assembling 100 HVBs for further validation inside chamber (to start when pin protections arrive, next week).
- Place next orders for all components.
- Order and ship "asap" larger quantities to IHEP, to ensure smooth assembly at IHEP under any condition. (Avoid risk of becoming more critical due to delays.)
- Assist IHEP starting to assemble ~1200-1400 monthly.
- Make provisions (e.g. HV systems) to avoid/minimize constraints among independent groups when retrofitting HVB_v5 into chambers .

PADC - Pressure ADC Board

• The PADC board digitizes the output from the on-chamber pressure sensors (incorporated in gas manifolds at front and rear of chamber). Is a 10-bit ADC + I2C link.

• 1 PADC/chamber; located in box at rear of chamber.

• Has local voltage regulator and current protection.

• All 250 units (plus spares) assembled.

• Currently passing QC & calibration.

• 50 units shipped to CERN, further 50 units arriving next week.

• Description on how to install the PADC is at http://www.physik.rwth-aachen.de/~reithler/040907PADC_installation.pdf

A PADC board in its housing box, ready for installation.

• Similar updated description for gas manifolds is at http://www.physik.rwth-aachen.de/~reithler/040731DTGasManif.pdf

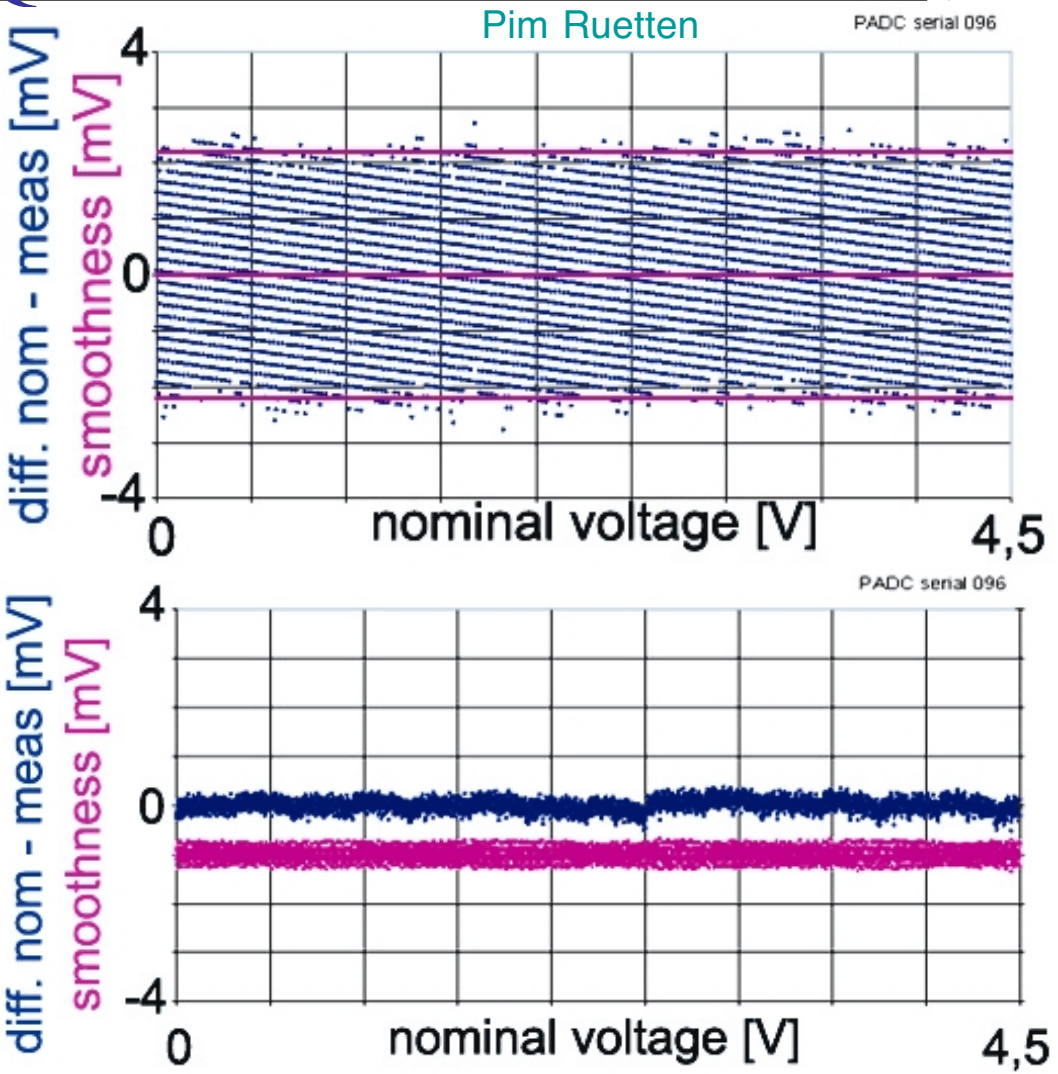
PADC QC & Calibration

METHOD:

- QC: check that every channel is working well for every input level.
- Calibration: determine the precise relationship between input level and digitized values.
- The measurement is repeated for every channel of the PADC.

RESULTS:

- QC: no failure found so far.
- Calibration: response is very linear; extract 2 parameters from diagram.
- Parameters are different for each diagram (corresponds to a high-resolution measurement of the input resistor network..)
- Done for 100 PADCs already.



QC and calibration of a PADC board. At top readings from the PADC, at bottom with higher resolution from the calibration bench. At top see digitization pattern; before calibration this band appears slightly inclined.