Drift Tubes Chambers
L1 Trigger

Emulator Status and Test:

- Bench tests
- Test beam 2003

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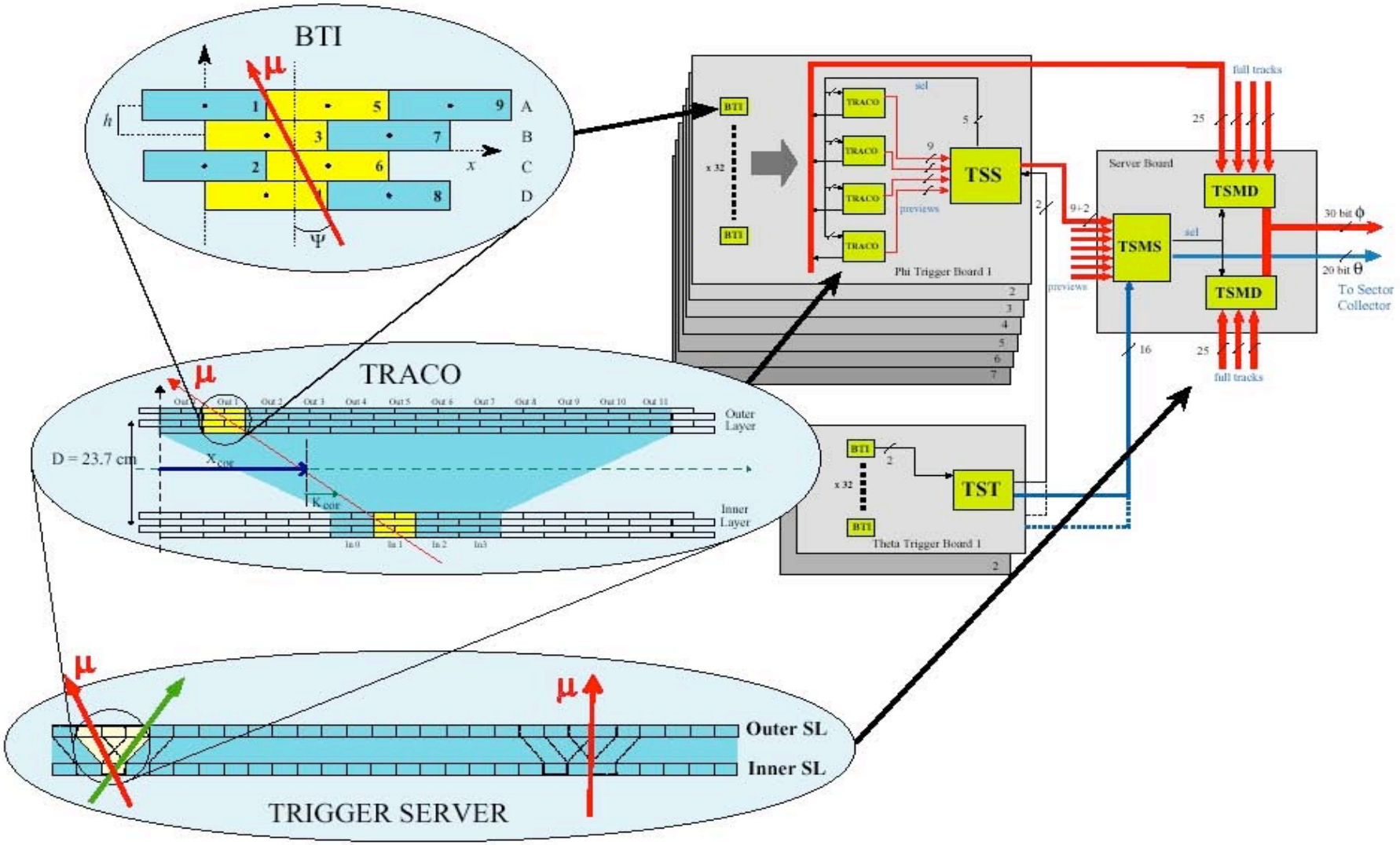
Topics:

- hints about L1 trigger hardware
- test bench performance
- trigger emulation with test beam data
- conclusions and future plans

1 Level Trigger



10^9 interaction every second → 100 kHz to the High Level Trigger

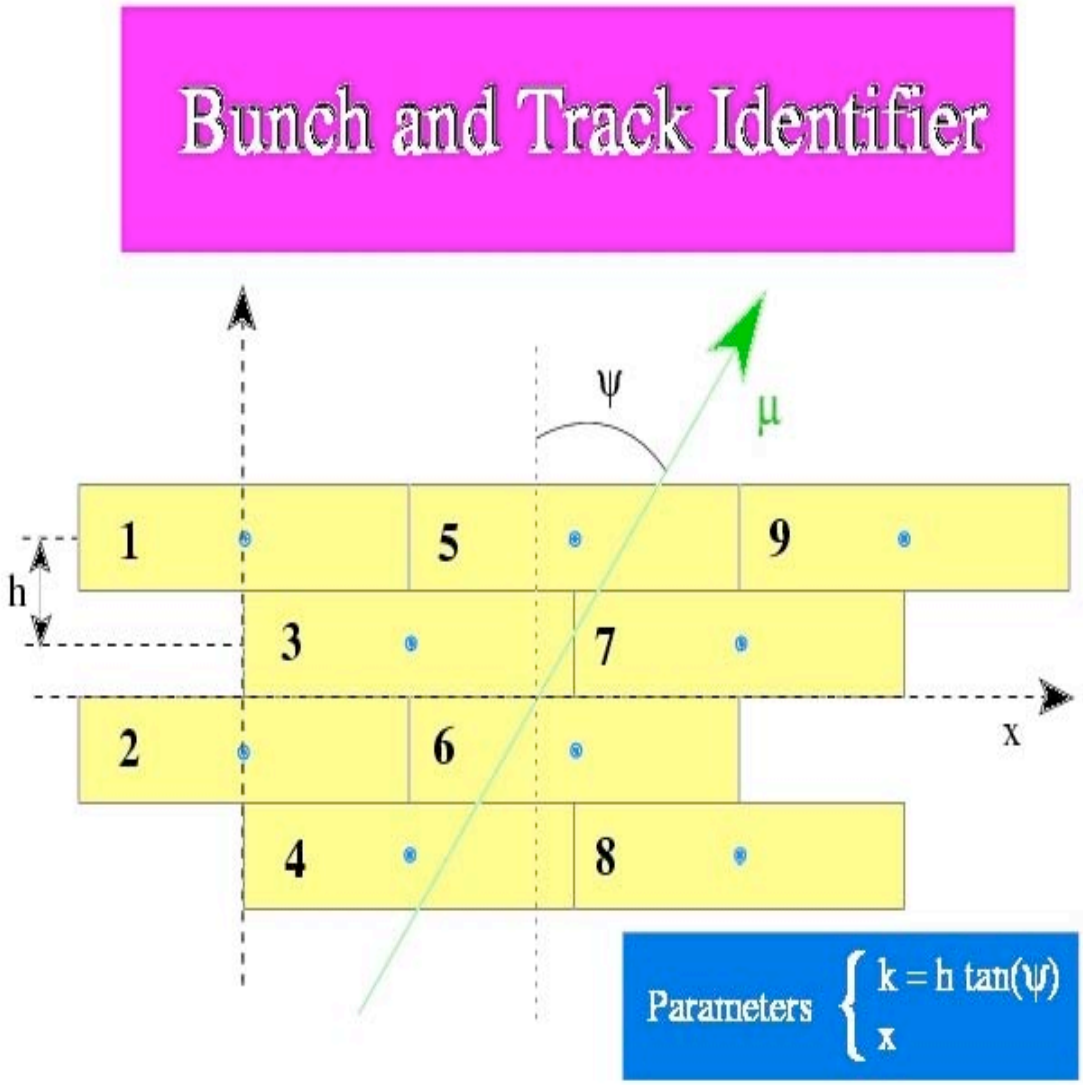
Bunch and Track Identifier

40 MHz cycle:

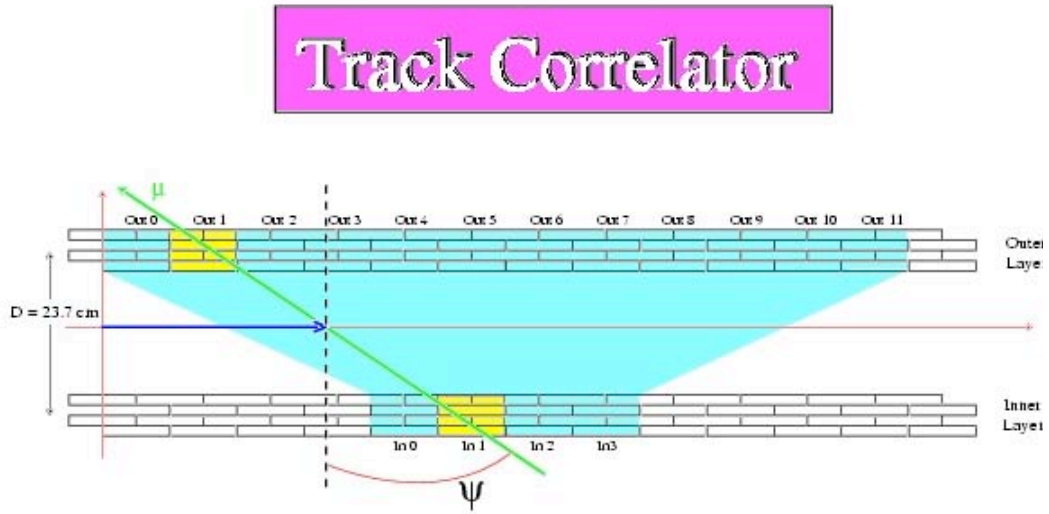
***INPUT*: 9 wires front-end signals**

***OUTPUT*:**

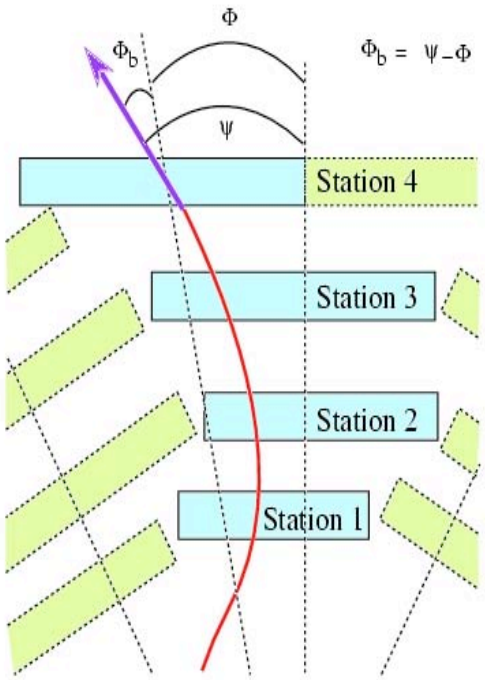
- ***X* position parameter** *(6 bits)*
- ***K* direction parameter** *(6 bits)*
- **bunch crossing**
- **trigger *type*:**
  - HTRG - 4 hits alignment
  - LTRG - 3 hits alignment



TRACO



Correlates BTIs in the inner and outer Superlayers
Refines the track measurement
(angular resolution 60 mrad ➤ 10 mrad)
Applies noise filtering



Output parameters

Radial angle Φ (12 bits)
Bending angle Φ_b (10 bits)
Quality flags

INPUT:

- 4 inner and 12 outer BTI triggers

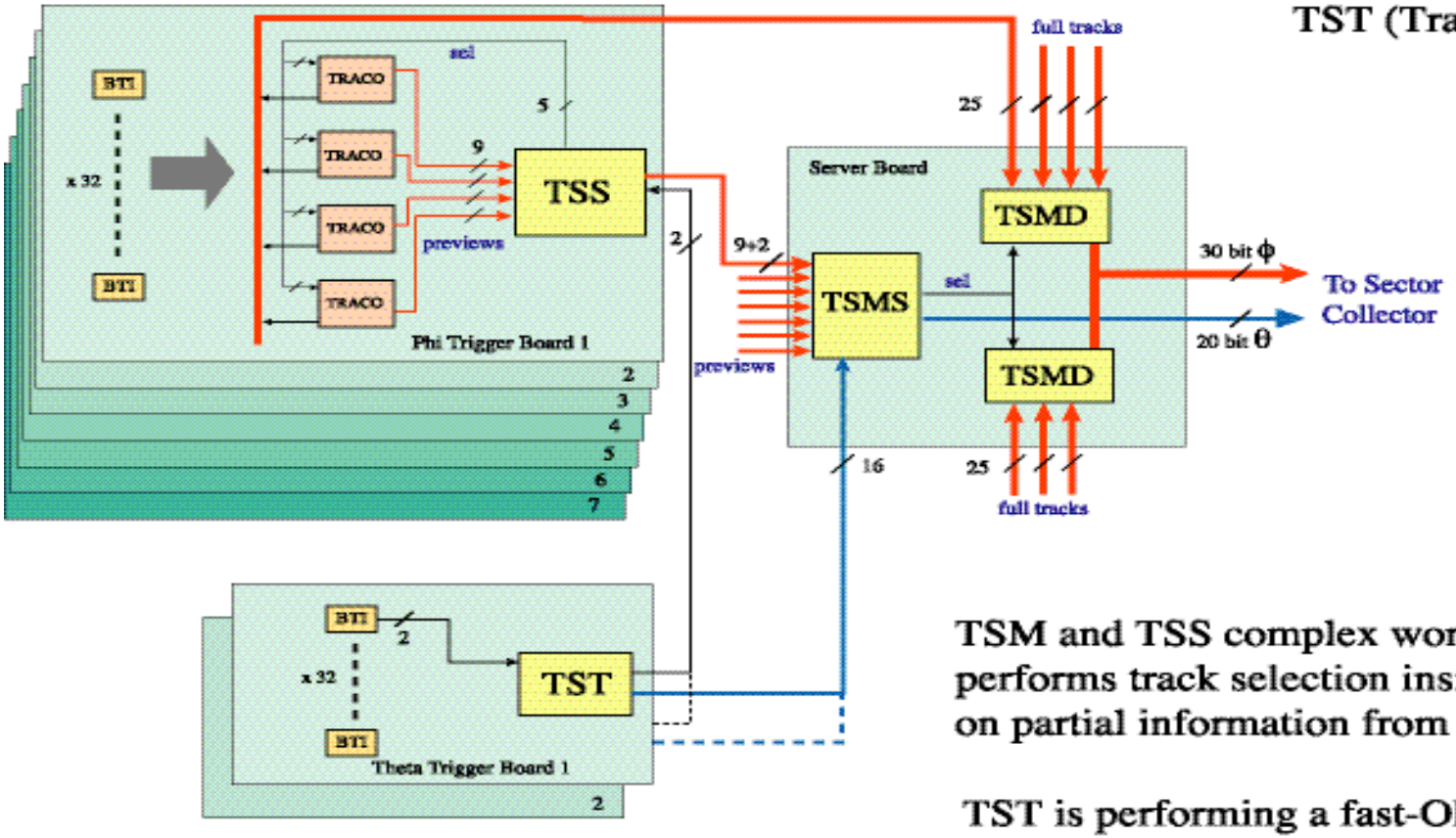
OUTPUT:

- X and K parameters of I and II track in CMS frame (radial and bending angle)

- trigger quality code: correlated HH, HL, LL and uncorrelated

Trigger Server

Trigger Server Architecture



Server system is divided in three parts
- TSM (Track Sorter Master)
- TSS (Track Sorter Slave)
- TST (Track Sorter Theta)

TSM and TSS complex works on the bending plane: performs track selection inside one chamber working on partial information from TRACO (preview)

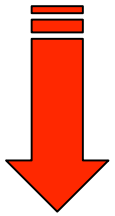
TST is performing a fast-OR of BTI signals in the longitudinal view for TRACO triggers validation

Sorts 2 best track candidates per clock within each chamber and suppresses ghosts

BTI and TRACO test on bench

BENCH TEST SETUP:

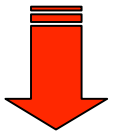
- BTI or TRACO chip
- input pattern unit and an output pattern unit
- pc for pattern unit read and write operations through data interface



It’s possible to :
inject every possible pattern stream in every possible setup,
analyse output pattern stream **to test chip functionality** and performance

BTI and TRACO emulator

Using bench test with a well working chip it's possible to:
compare hardware output stream with chip emulator output



GOAL : obtain an emulator reproducing the hardware at 100%:
every bit at every clock for every setup

Emulator code:

FIRST EMULATOR CODE:

Single chip standalone emulator from ORCA_4 L1 Trigger package (Claudio Grandi).

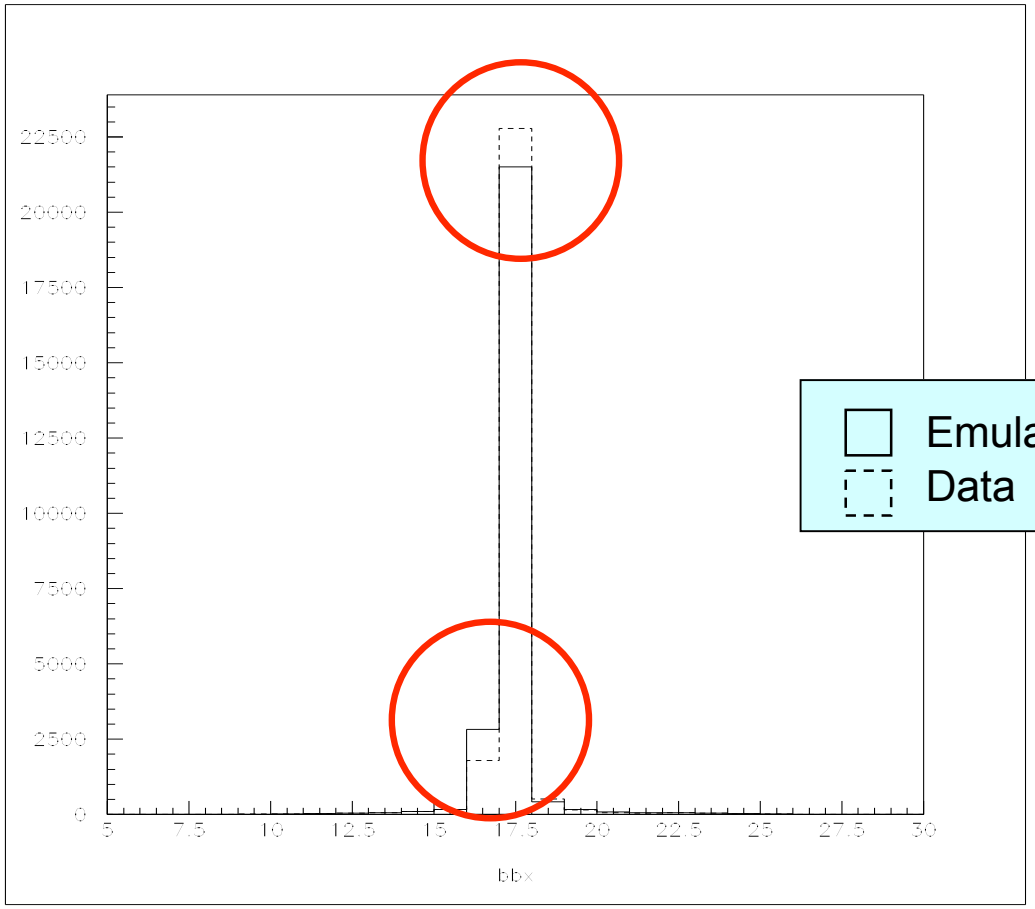
SITUATION:

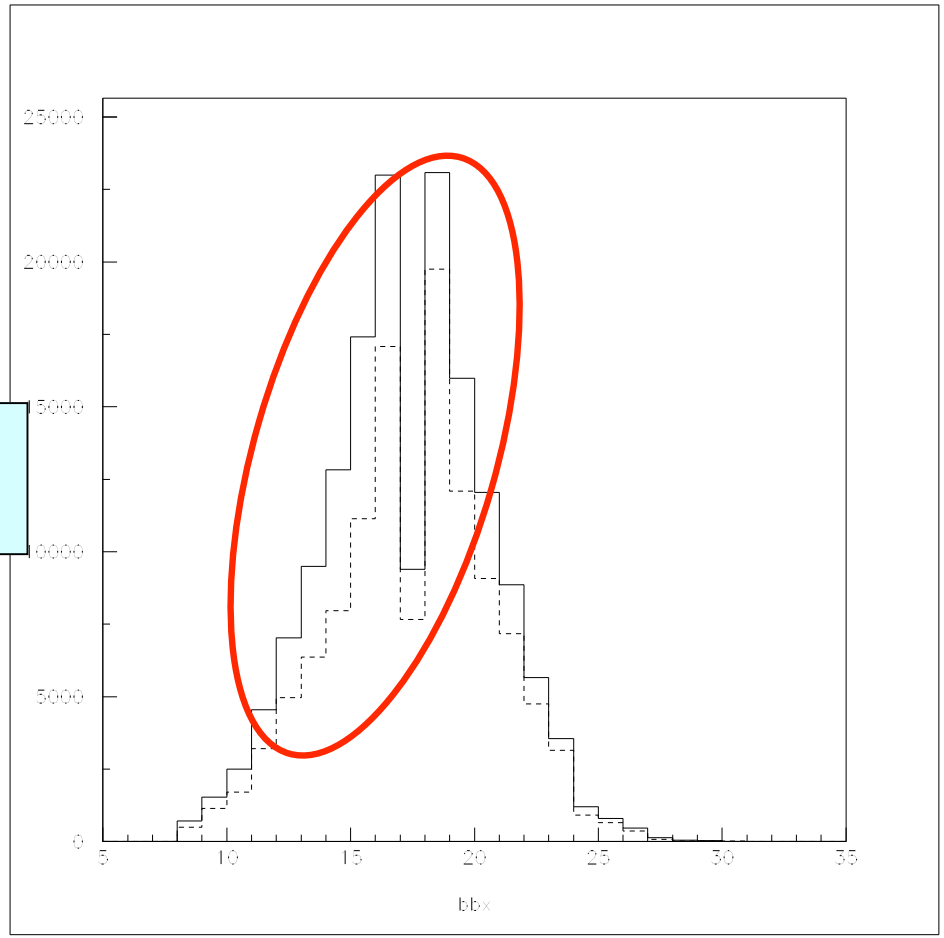
- missing parameters:
  - redundancies-ON and X-type patterns-ON mask added
  - trigger DEAD time for wires implemented
  - pattern masks added
  - wire masks added
- incomplete or incorrect algorithms
- difficulty to understand behaviour of a chip that works on several bunch crossings

PROBLEM: missing or incorrect documentation about some chip features! Exact algorithm not described.
Need to deduce exact chip algorithm from:

- working/not working event classification

BTI output trigger distribution





H triggers:

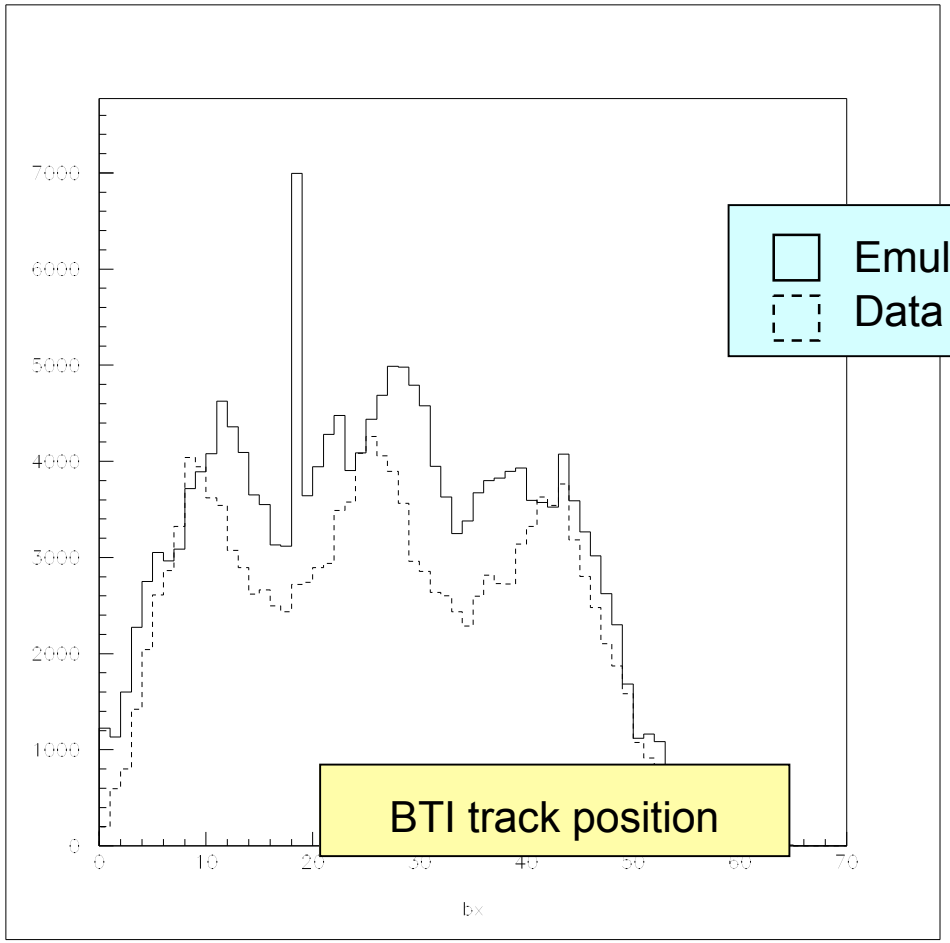
- 6% missing H trigs in time
- 4% H out of time

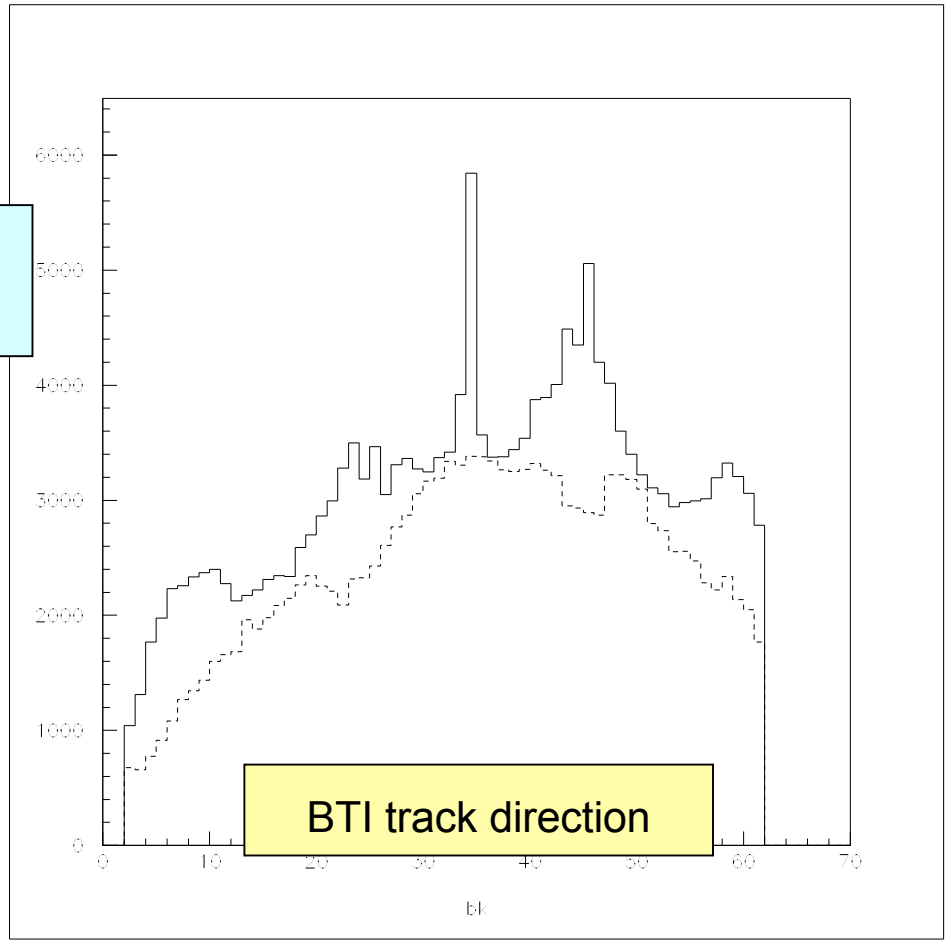
L triggers:

- 30 - 50 % excess L triggers in simulation

MUST analyse every single event at time !!!

BTI X and K distributions





Improvements examples:

- int algebra in K and X computation equations with remainder of divisions computed according to particular/non-intuitive tables

- shift register value range fixed

- low triggers fixes:

  - only one K reference value!
  - X equation choise for particulare cases
  - K range acceptance for A and D low +-1 and +-2 for B and C low trigger types

TRACO emulator

SITUATION: simpler behaviour: as for BTI, we deduced algorithms from hardware output.

SOME ADDED FEATURES:

- Low Trigger Suppression (add some flags as LVALIDIFH)
- parameter configuration and LUTs from hardware setup file

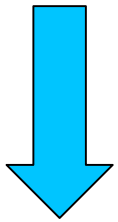
SOME IMPROVEMENTS:

- Low Trigger Suppression fix:

  - 4 bx before H and 1 bx after (for both I and II track)

  - applied after bending angle cut
- Reuse of BTI triggers for II track fixed (only if I track is accepted)
- fix 2nd track overlap code

After implementation of all these corrections



100 % agreement
hardware = emulation
on test bench
for every bit
at every clock
and every configuration

L1 trigger emulation code in ORCA
for testbeam data comparison

BTI:

TRACO:

TS:

code released in orca_7_5_0

October 2003

+ emulator updated (verification in progress)

REAL DATA INTERFACE:  *at the moment private code !!!!!*

- .orcarc parameters from hardware (BTI and TRACO) setup interface
- Look Up Tables (X,K---> CMS frame) from hardware setup
- flat file input: raw data unpacking, store MuBarDigis (Paolo Ronchese - implementing Giacomo Bruno DaqOnLine code for next testbeam release)

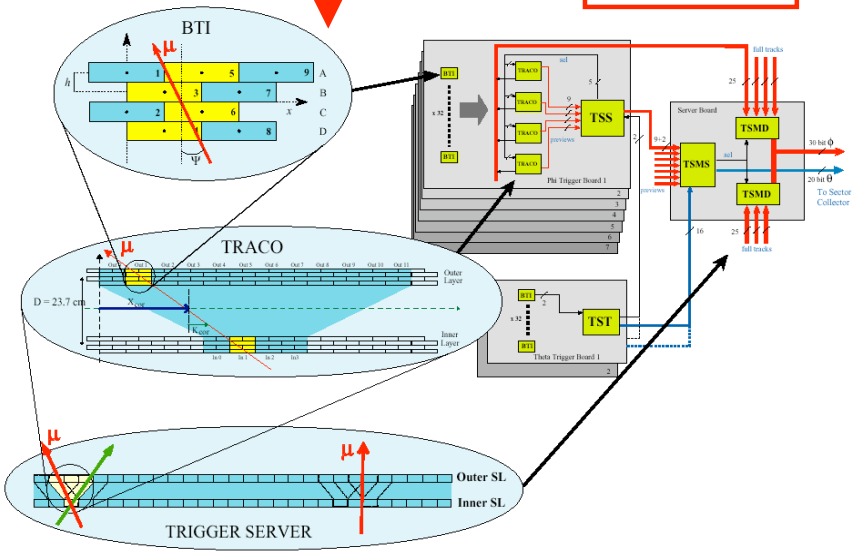
Preliminary tests : needs more work to verify

TB2003 Hardware

front-end signals

charge preamplifier
shaper
discriminator

TDCs



2 segments in R-phi view

ORCA721_TB03 Simulation

TBApplication:
-Reads file
-Dispatchs TBEventProxy (bit stream)

DAQ flat file

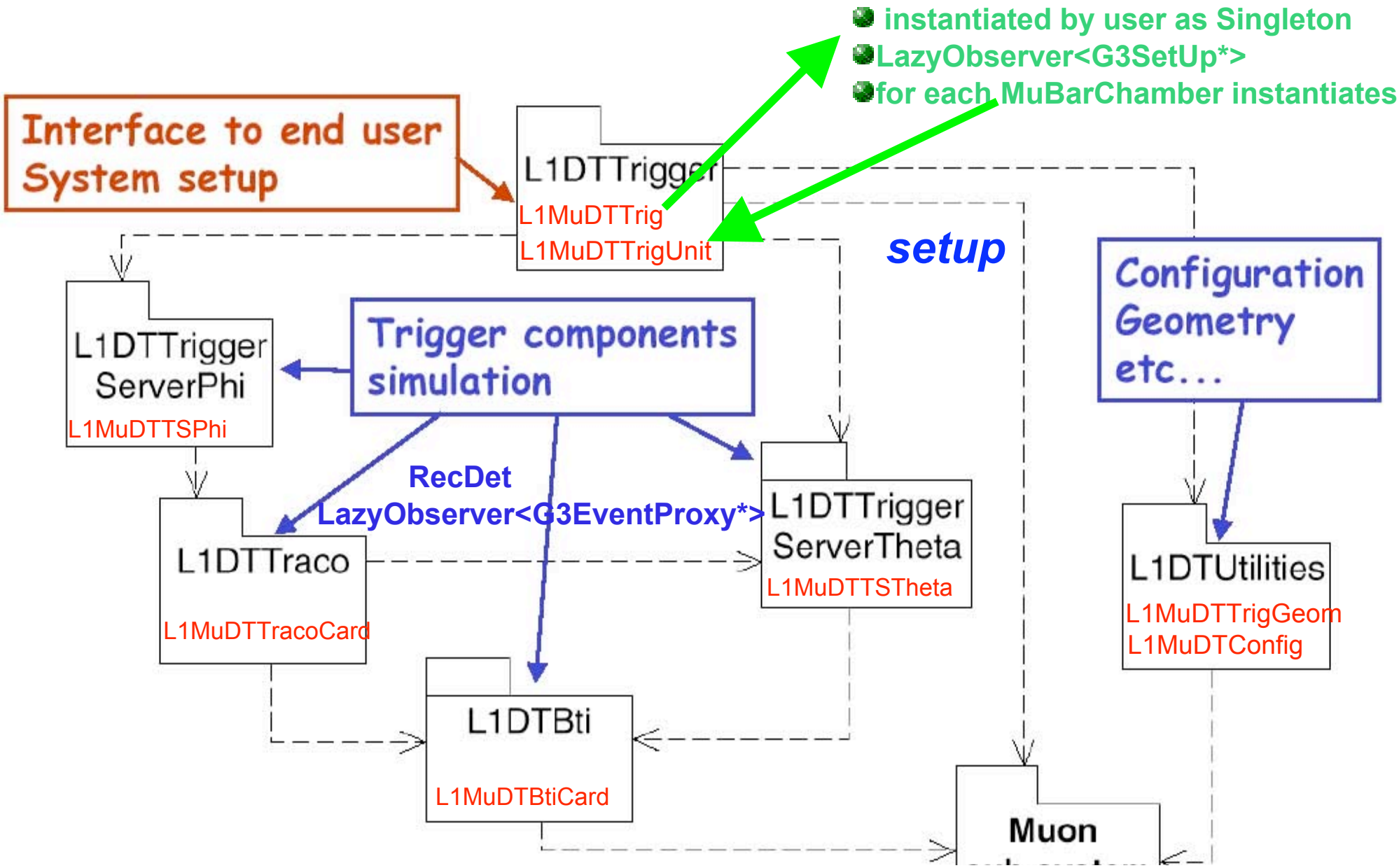
DTBXReadout → MuBarBaseReadout → MuBarDigis

TB private code

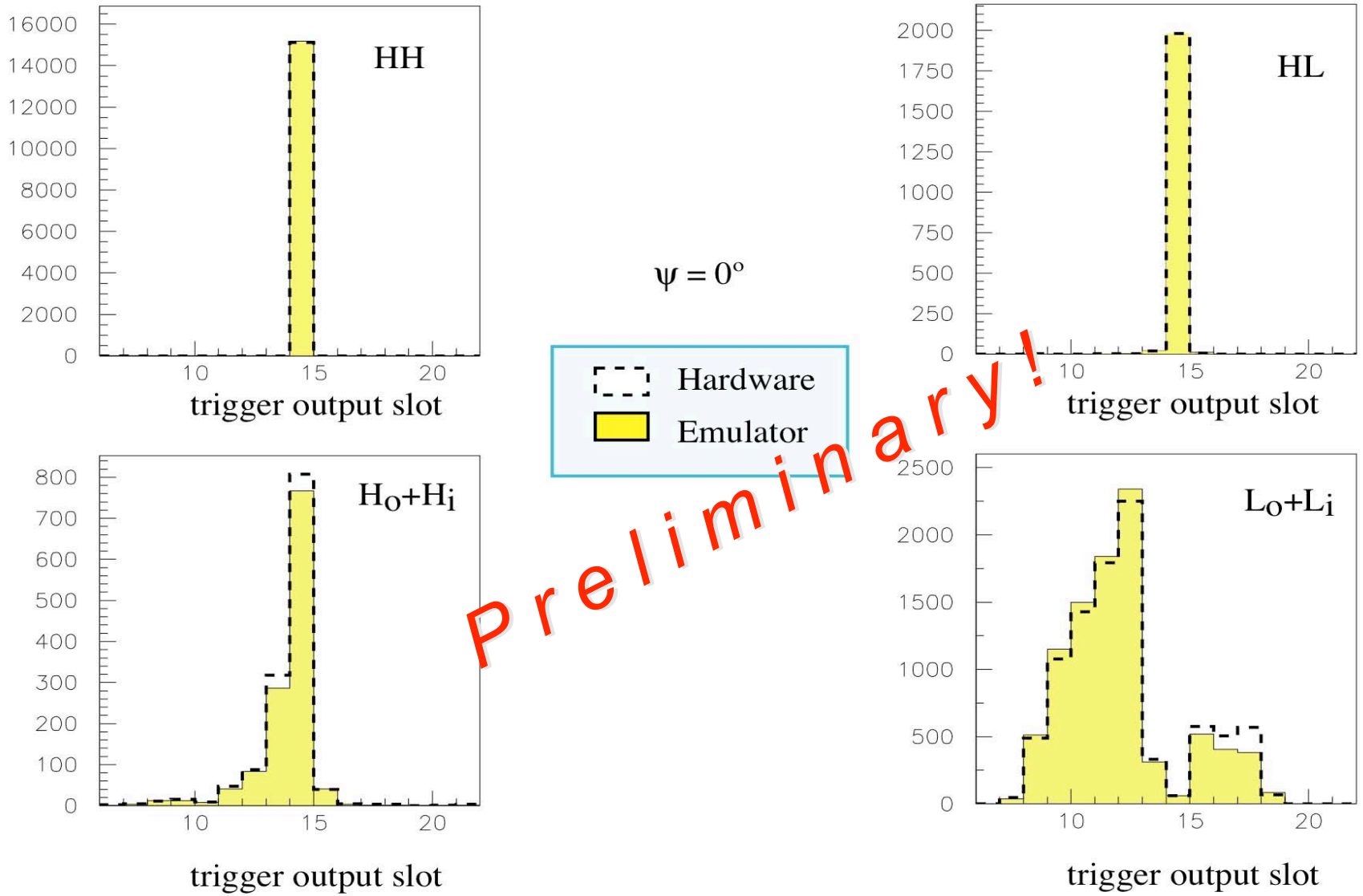
ORCA **Trigger** package
L1DTBti
L1DTTraco
L1DTTriggerServerPhi/Theta

L1MuDTChambPhSegm

ORCA L1 Trigger Packages

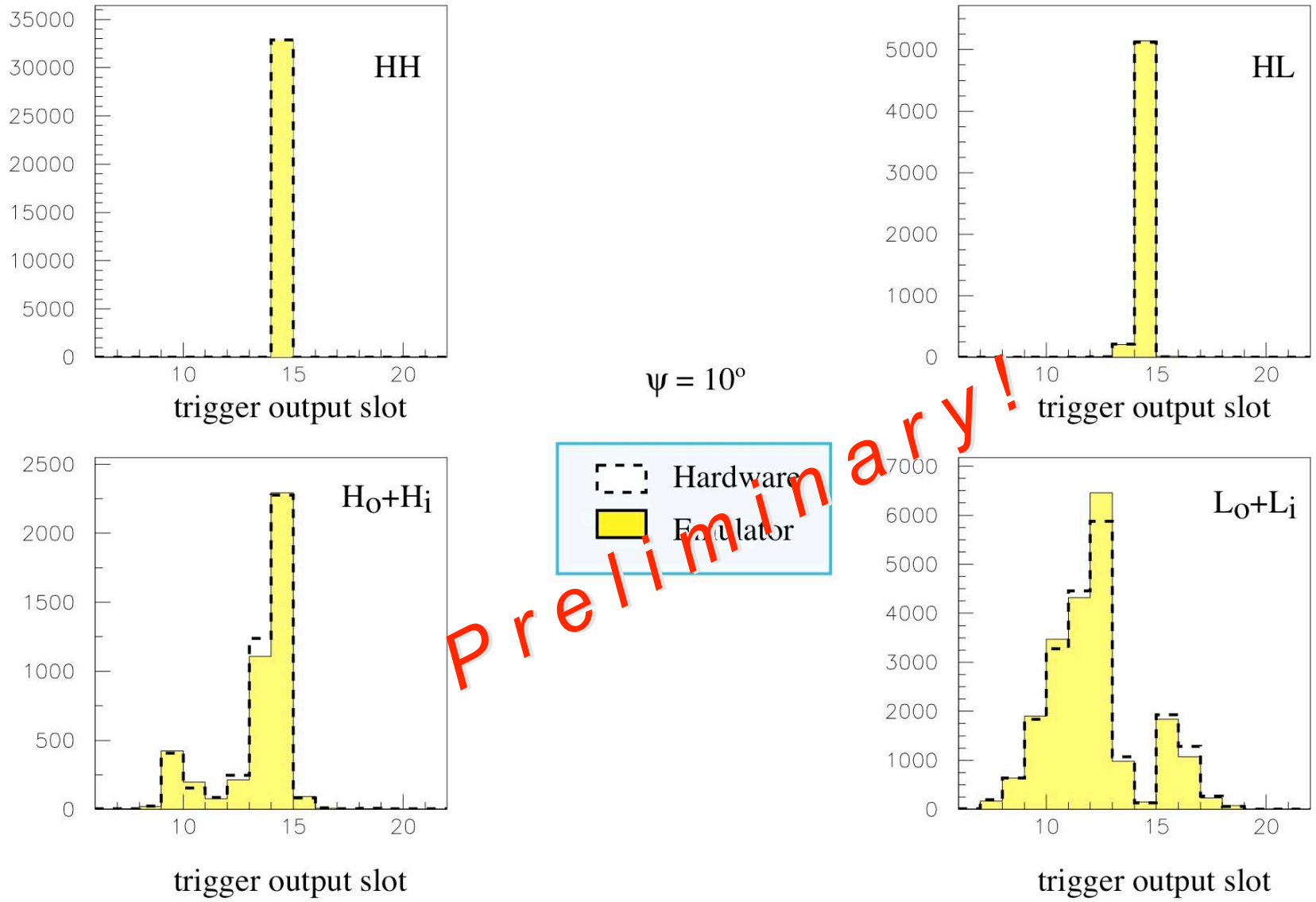


Single muons trigger distribution - 0°

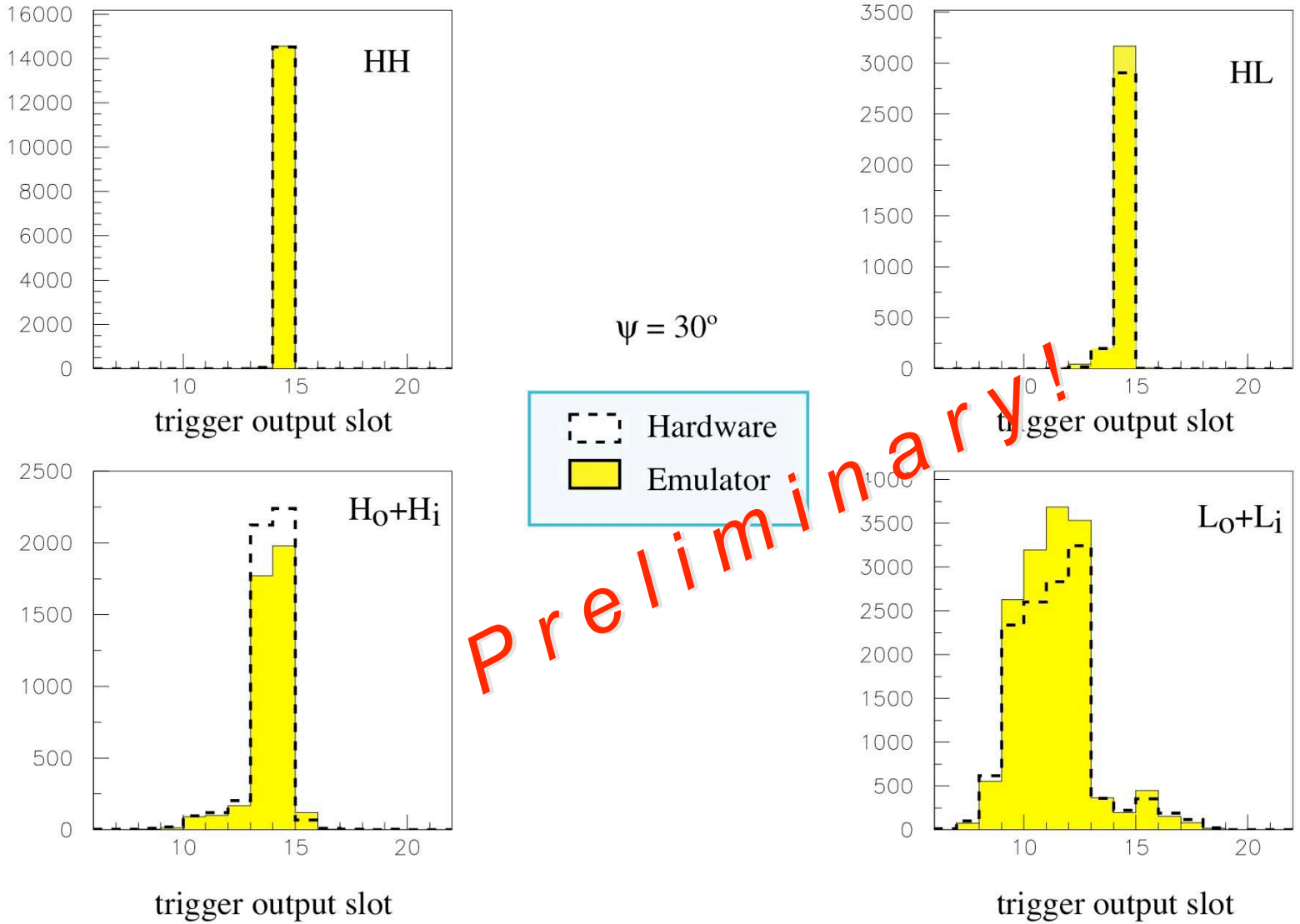


→ very good agreement for correlated triggers HH HL bx distribution

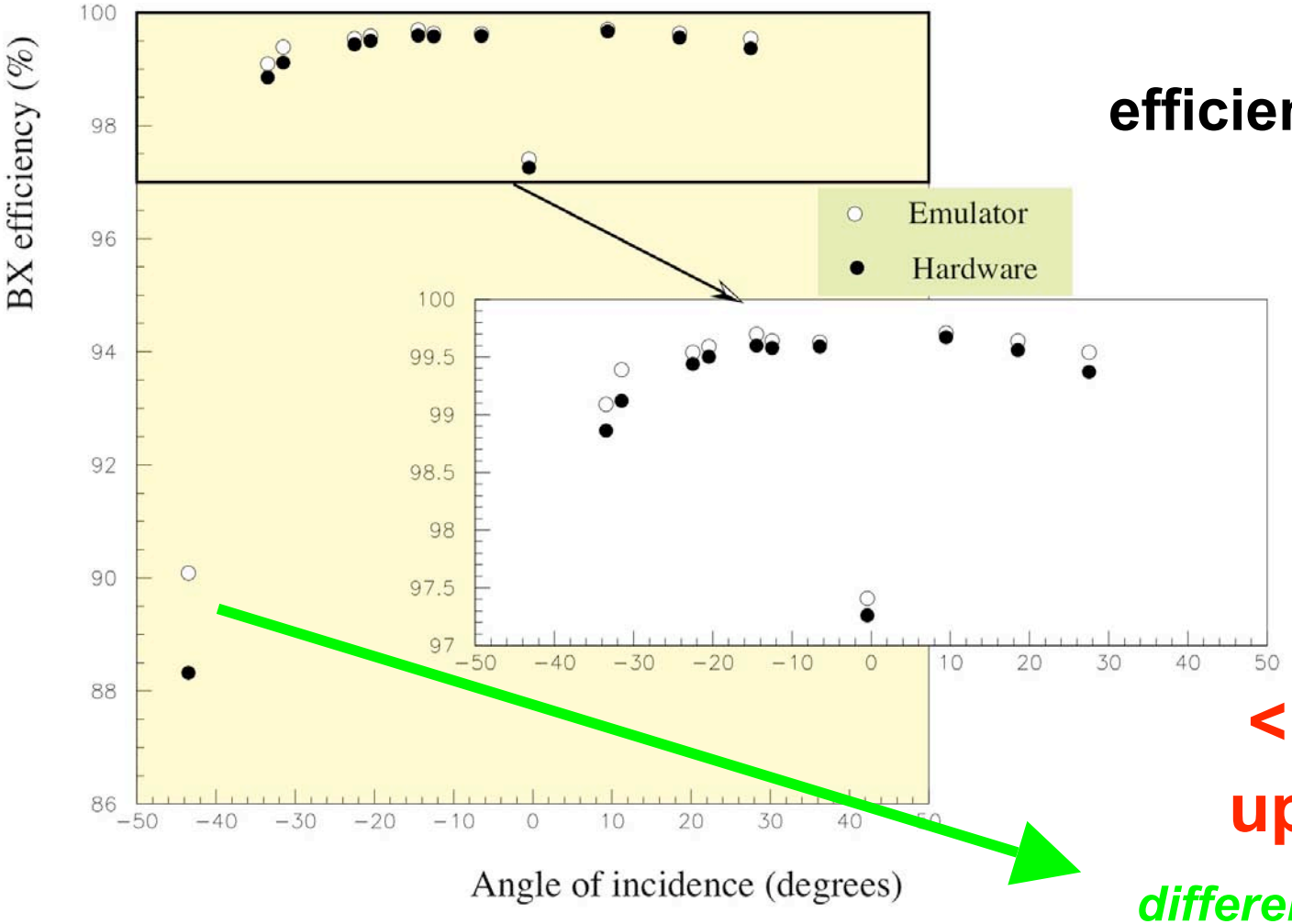
Single muons trigger distribution - 10^0



Single muons trigger distribution - 30^0



BX Efficiency vs Incident Angle

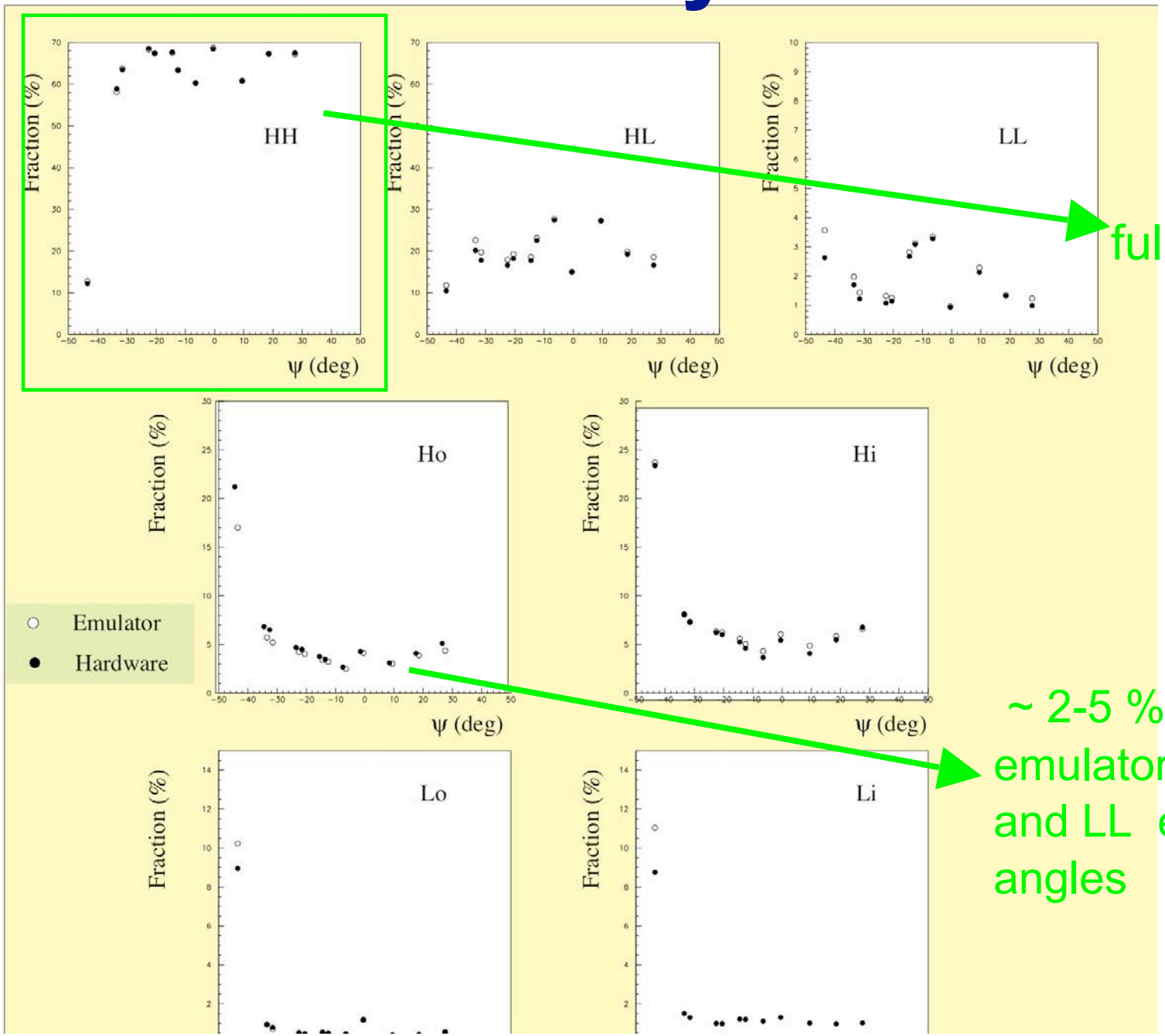


$$\text{efficiency} = \frac{\text{trig. right bx}}{\text{scint. trig.}}$$

<1 % differences up to 35^0

differences may be associated to still not correct implementation

BX Efficiency for each trigger type

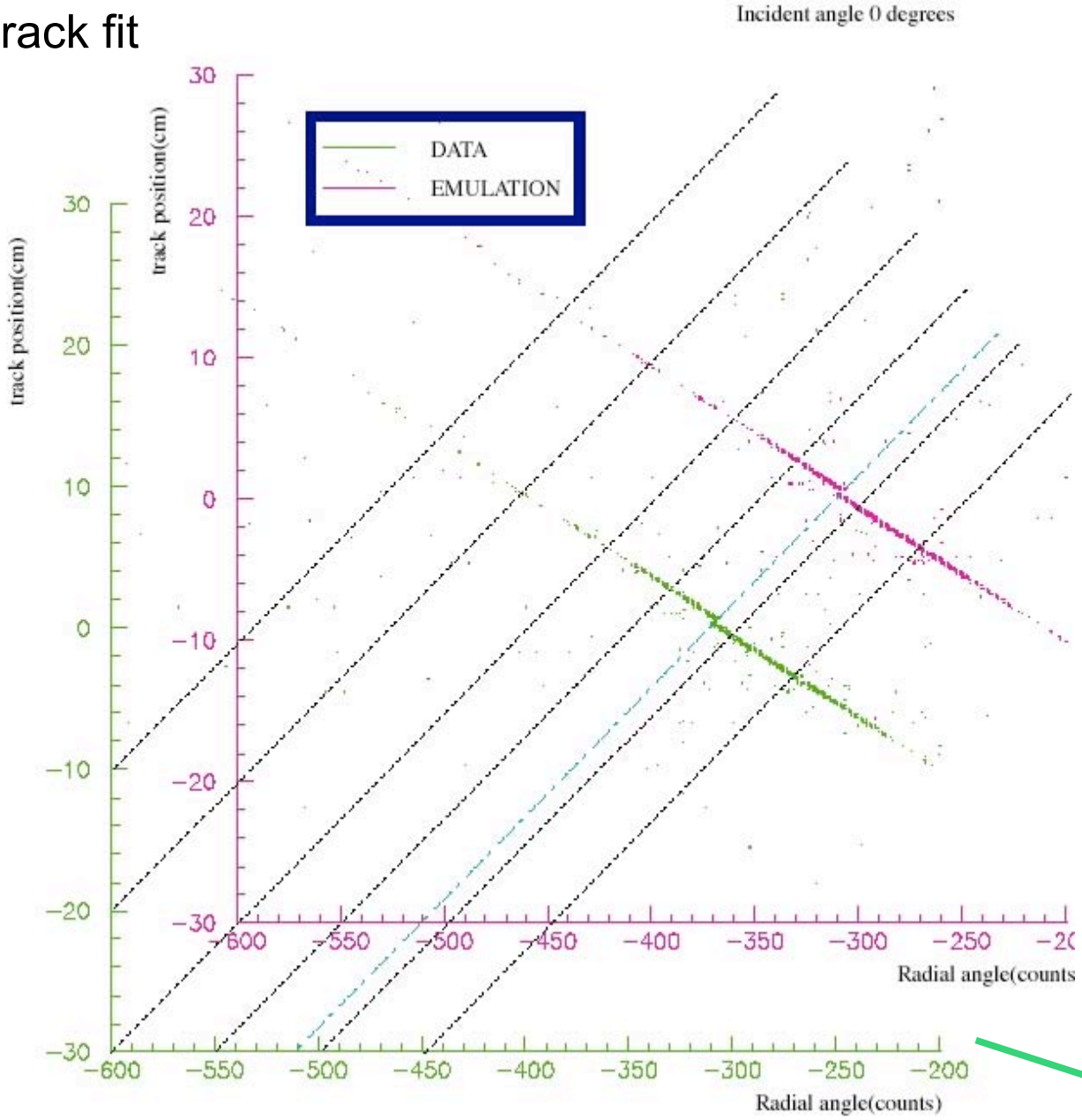


full agreement for HH

~ 2-5 % Ho trig deficit in emulator compensated by HL and LL especially at large angles

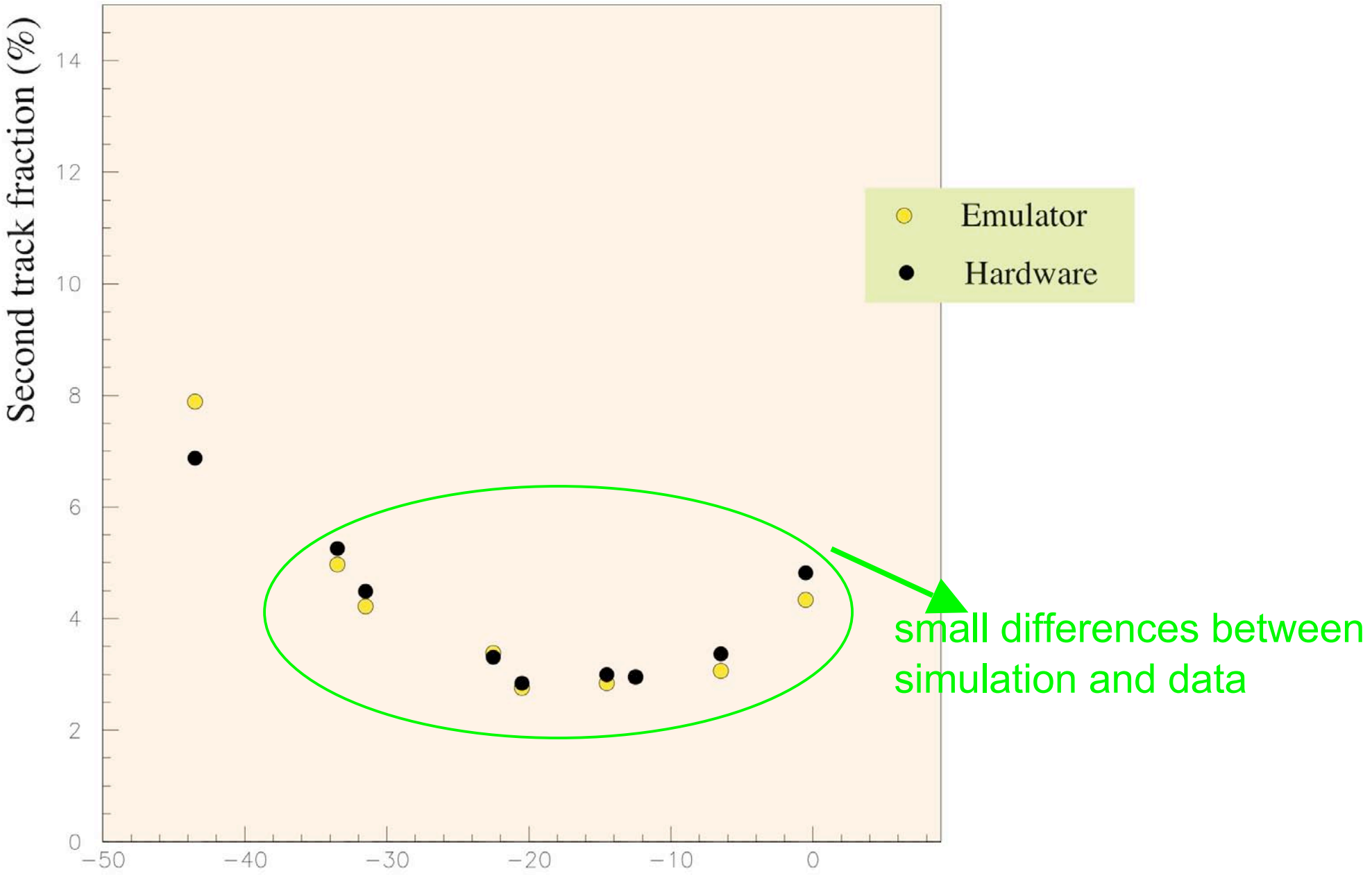
Fitted vs Trigger Track Position: emulation - data comparison

ORCA track fit



ORCA trigger output

In time noise



Comparison of performance for different configurations

OK

fix

0°	Configuration					
	Default	L accepted if Hθ	L rejected	BTI LTS off	TRACO LTS on	TS ghost rejection off
efficiency	82.36	87.60	81.66	81.77	80.70	82.18
	82.37	87.70	81.68	81.77	80.75	82.18
in-time noise	2.84	3.65	1.28	0.84	1.71	57.16
	2.51	3.44	1.20	0.32	2.24	57.36
off-time noise	50.67	15.14	8.11	190.79	24.63	61.02
	52.20	34.65	8.86	192.83	33.90	115.76

OK

fix

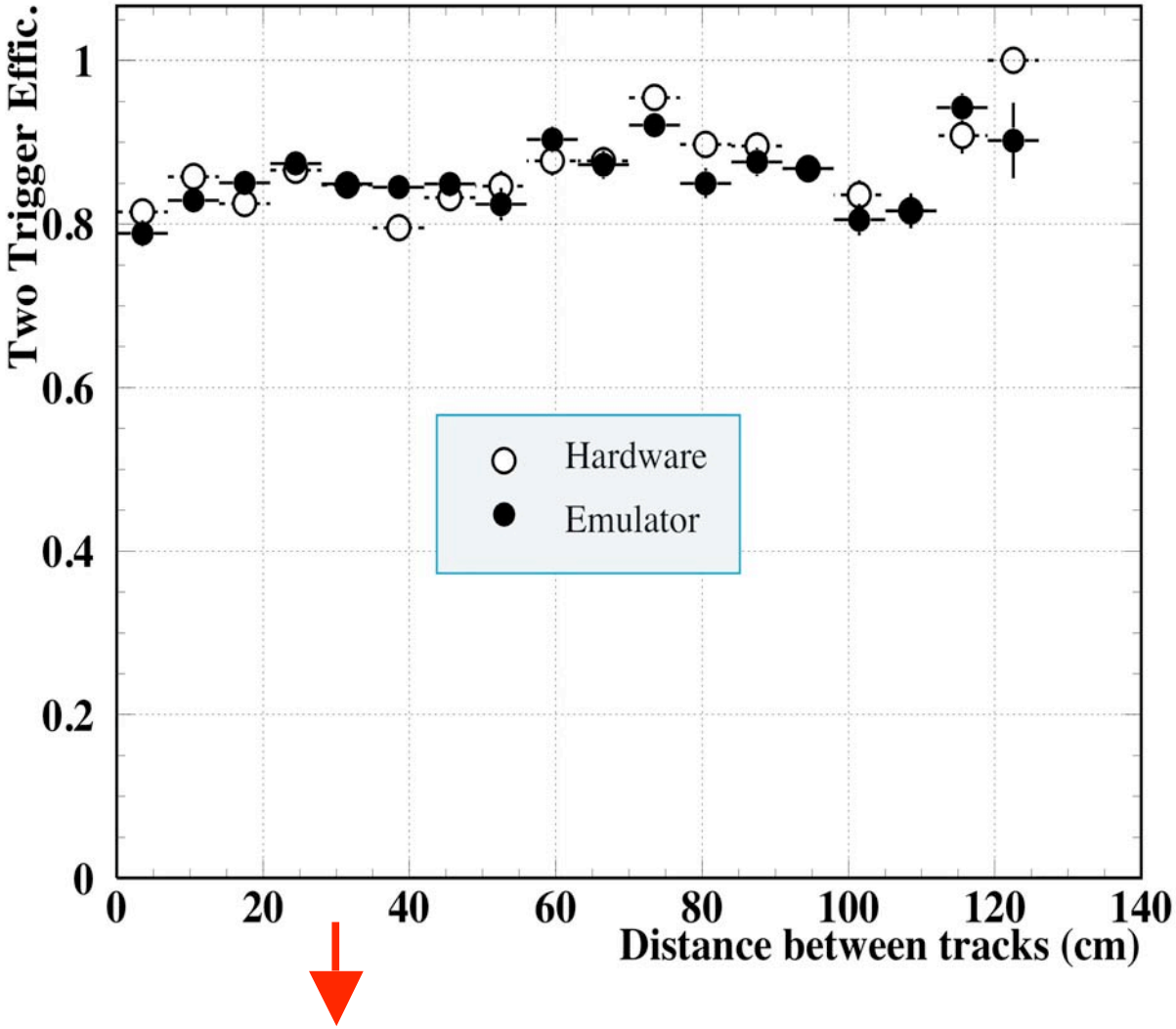
30°	Configuration					
	Default	L accepted if Hθ	L rejected	BTI LTS off	TRACO LTS on	TS ghost rejection off
efficiency	88.10	87.60	86.50	87.79	87.17	87.82
	88.22	87.70	86.63	87.81	87.75	87.93
in-time noise	3.45	3.65	2.00	2.06	2.64	27.26
	3.83	3.44	1.90	0.53	3.30	27.70
off-time noise	72.20	15.14	14.60	202.23	38.48	81.81
	100.65	34.65	33.38	271.34	41.87	138.05

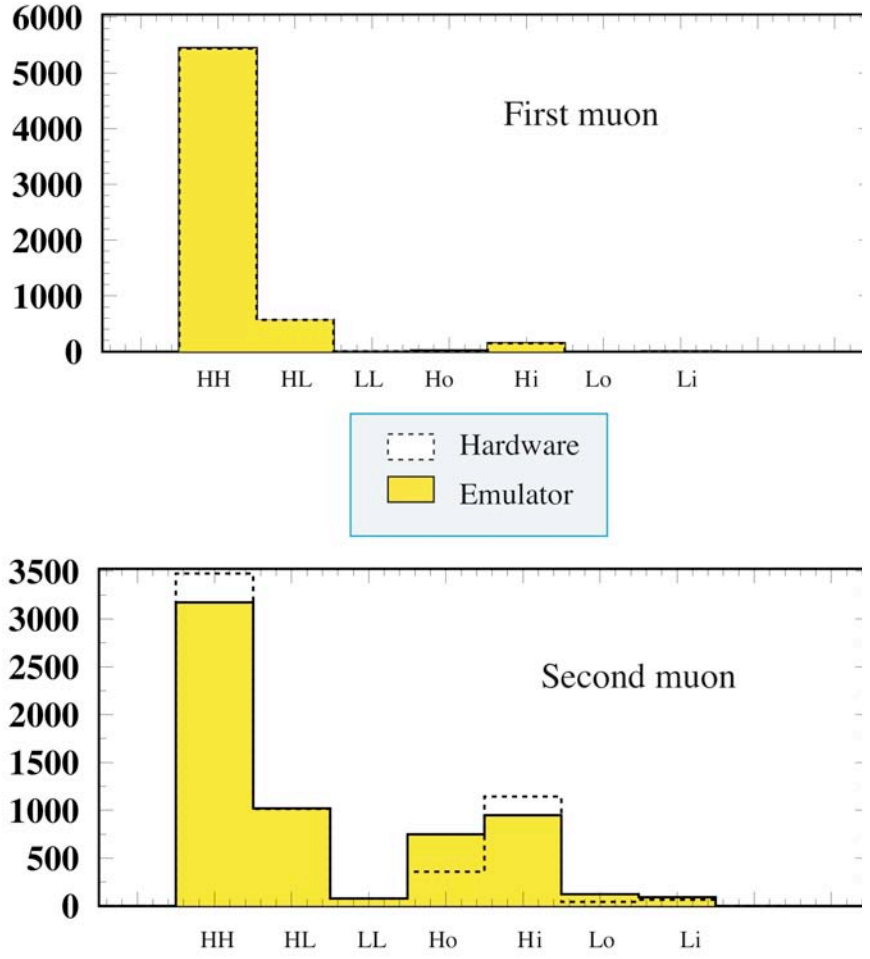
Hardware

Emulator

to give suggestions of the work to do: efficiency and in time

Two muons sample (Stefano Marcellini et al.)





fluctuations due to poor

10% deficit for 2nd muon of emulated

HH compensated by Ho: dead TDC

…for a better agreement…

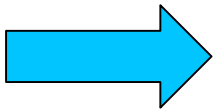
- verify the correct implementation of BTI and TRACO emulator algorithm in ORCA (fix and debug!)
- verify that the relations between BTIs, TRACOs, TRIGGER SERVER in a emulated chamber works properly
- emulator trigger input are TDC data, NOT trigger input: need to tune input conversion ! (similar to hardware syncronization)
- take into account hardware malfunctioning (e.g. TDC dead channels ….)

Conclusions and future plans:

IN THE SHORT RUN…

- fix testbeam data comparison incongruence
- release fixed code in ORCA_8
- write exhaustive BTI and TRACO documentation

IN THE LONG RUN… be able to TUNE CMS TRIGGER PARAMETERS TO GAIN HIGHER EFFICIENCY AND LOWER NOISE!



using EXACT Trigger Board emulator

study and optimize CMS trigger performance

in the real expected CMS situation, e.g.: - noisy and dead channels

- wide angle distribution