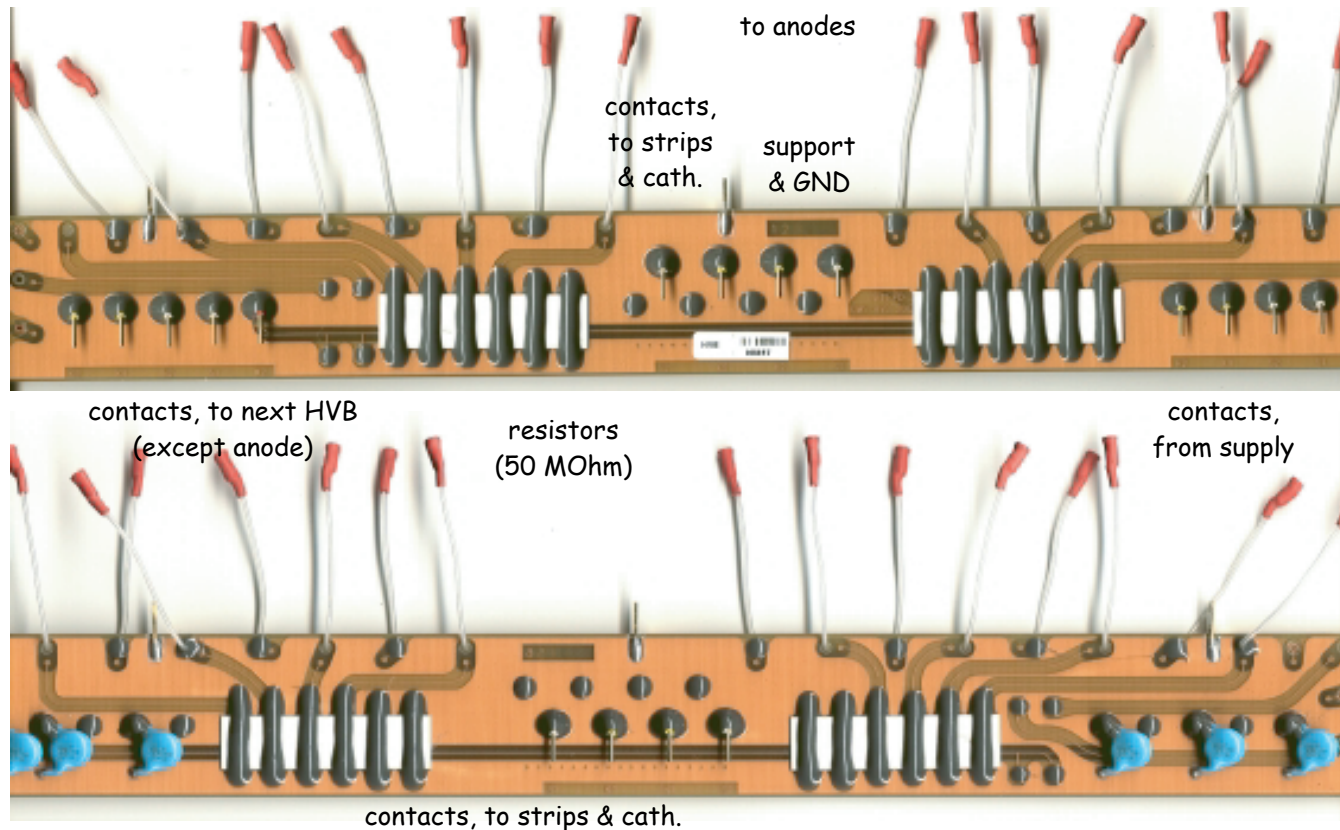


DT CHAMBERS: Layout of HV distribution board “HVB” - from HVB_v1,... to HVB_v5 -

Recent work by Enrico Borsato, Guenter Hilgers, Hans Reithler and Piero Zatti

Hans Reithler
040316

HVB Structure & Function

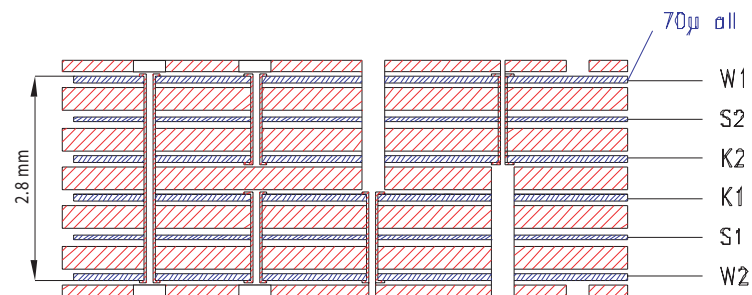


Top and bottom view of an HVB_v1.

It is a HV distribution board for up to 20 drift cells:

- 6 independent voltage channels from the supply (2 for anodes, strips and cathodes) ; strip and cathode voltages are passed to the next HVB for coarser granularity.
- 24 resistors (1 per anode and 1 per 10 strips and 10 cathodes).
- 6 capacitors (1 per HV channel)
- daisy-chain cables to strips and cathodes (not shown)
- 6-layer PCB; path for each voltage channel in one layer; innermost layers for cathodes, outer layers for anodes.

capacitors to GND (471 k/6 kV)



Schematic structure of the 6-layer HVB PCB. Some holes do not go through the full PCB (contacting different groups of strips and cathodes). The two at the right are for the wires to the anodes and serve also as protection for the connecting wires.

Version 1 (March 1999, "Original") :

Distance between track and GND ~ 1.6 mm in all 6 layers; for +3.6 kV anode it means ~ 0.45 mm/kV. Some assembled ones found nevertheless to fail after successful ~ 2500 h operations at nominal voltages. Suspicion has been that outer "pre-preg no flow" layer has bad adhesion and HV breaks down through some micro channels between PCB and pre-preg. HVB PCB shows discharge along surface and borders at ~ 11 kV; when covered stands ~ 15 kV (few hours; test ~ 040123 Pd).

Version 2 (November 2002, "Improved 1") :

Only outer layers (1 and 6) modified to increase the distance between track and GND to ~ 2.7 mm; for +3.6 kV anode it means ~ 0.75 mm/kV. Inner layers 2 to 5 still having ~ 0.45 mm/kV (for anode, via holes going through).

Version 3 (November 2002, "Improved 2") :

As v. 2, but with less GND on outer layers; incomplete layout; only sample exists.

Version 4 (February 2004; "Future 1") :

Enlarging spacing and distance to borders on all layers; removing most GND on outer layers, to reach 1.5 mm/kV within all layers and also between electrodes of different layers, along PCB borders. (See also further details on next pages.) The insulator layer on the outer layers is still under discussion (2 x pre-preg as current HVBs, or glue (to be tested), or no-solder plus pre-preg; see then v. 5)

Version 5 (February 2004; "Future 2") :

As v. 4, to reach 1.5 mm/kV everywhere. Move from 6 to 8 layers, to have better prepreg insulation on layers with 4 kV lines (are now inner layers). On outer layers have only pads for components; HV protection mainly by glue. Safest choice, for present understanding.

For comparison:

Test on an unprotected PCB surface: discharge at ~ 0.33 - 0.6 mm/kV (test ~ 040123 Ac)

Recommendations:

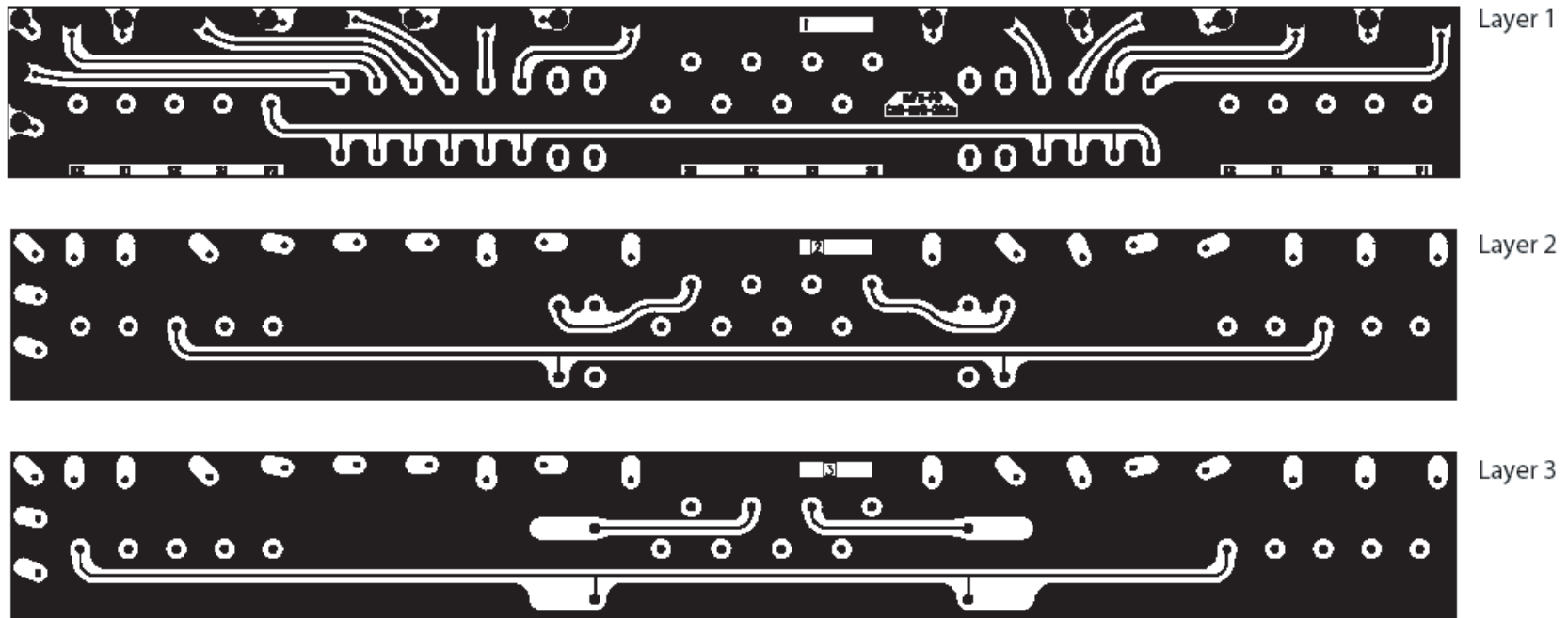
MIL-STD-2118 (1984): min. spacing on unprotected PCB 3.1 mm/kV, on encapsulated PCB 2.6 mm/kV

MIL-STD-275B (from Andus Electr.): min. spacing on unprotected PCB 7.6 mm/kV, on encapsulated PCB 5.1 mm/kV

CAD progr. Target: min. spacing on unprotected PCB 13-19 mm/kV, on encapsulated PCB 3.7 mm/kV

Top three layers of the HVB_v1 ("O", Mar. 1999):

HVB_v1 (Mar. 1999)



Top three layers of the HVB_v2 ("I"; Nov. 2002):

HVB_v2 (Mar. 2002)



Layer 1



Layer 2

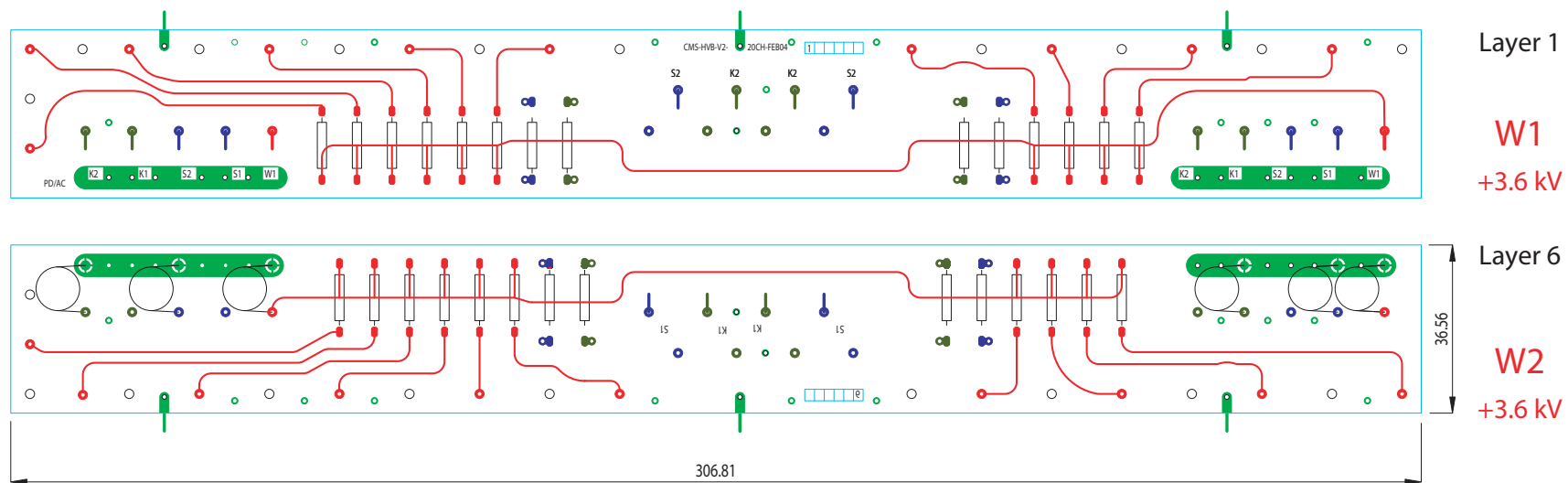


Layer 3

Only the outer layer differs from v1.

Proposal HVB v.4 Layout (I)

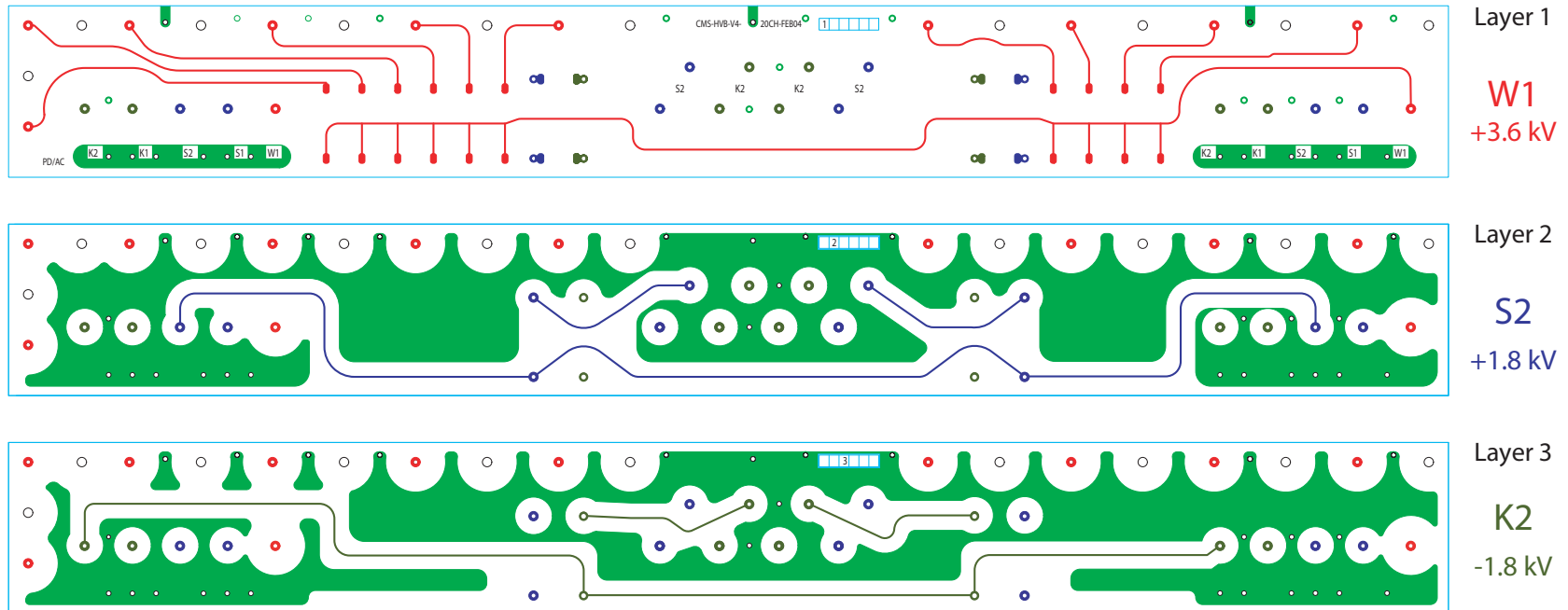
HVB_v4, view of assembled PCB:



Top three layers of the HVB:

The individual layers 1 to 6 of HVB_v4:

Color coding is related to applied voltages: **red** = anodes (+3.6 kV), **blue** = strip (+1.8 kV), **dark green** = cathode (≤ -1.8 kV), **light green** = GND.

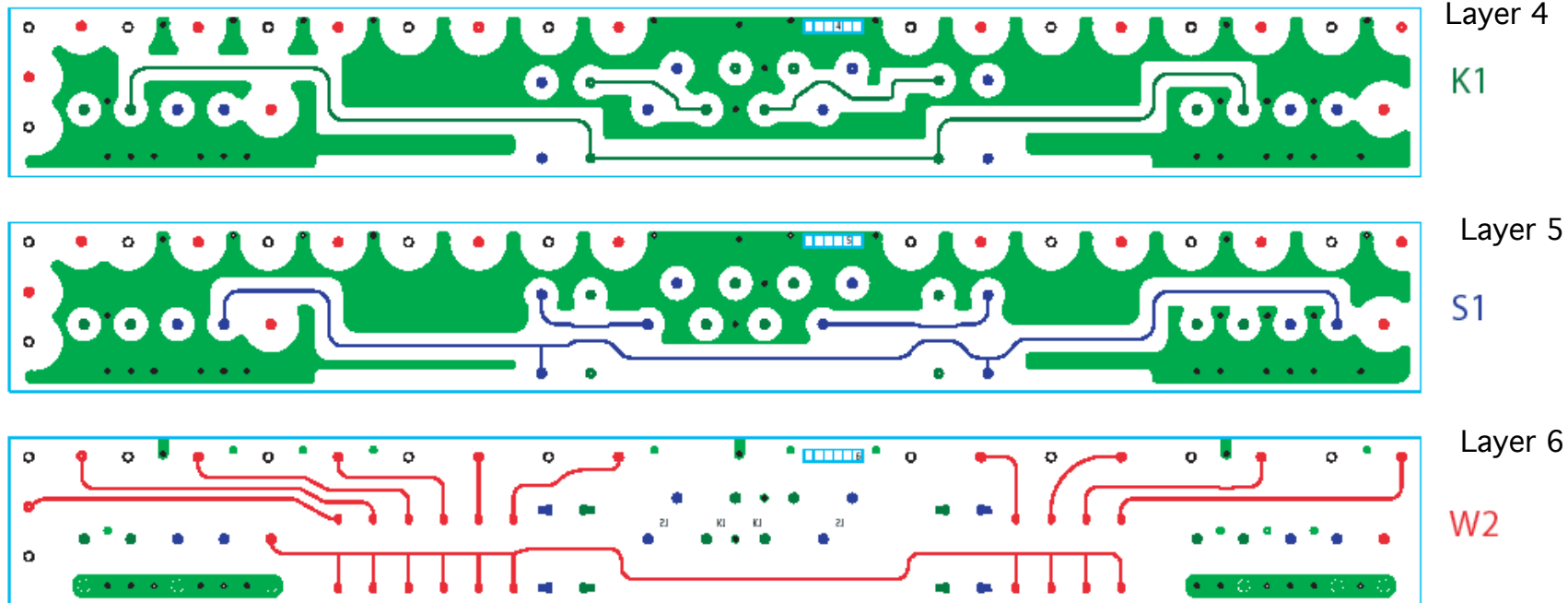


Remarks:

- 1- The number of layers, the logics of the circuit and contacts are unchanged, to be pin-compatible with existing HVBs and cables.
- 2- The plated-through holes for the Strip (S1) and for the Cathode (K1) resistors are through these 3 layers only (same for circuit on layers 4-6), while the holes for the Wires (W1), for all contact pins and GND are through the whole PCB. (Could assemble the two partial packages (layers 1-3 and layers 4-6) in a first step, and add a central prepreg and the outer prepreg layers in a second step.)
- 3- Size is 36.5 mm x 305 mm. The add. 1 mm in height to be checked.

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Bottom three layers of the HVB_v4:



Comparison of v4 with v1, v2:

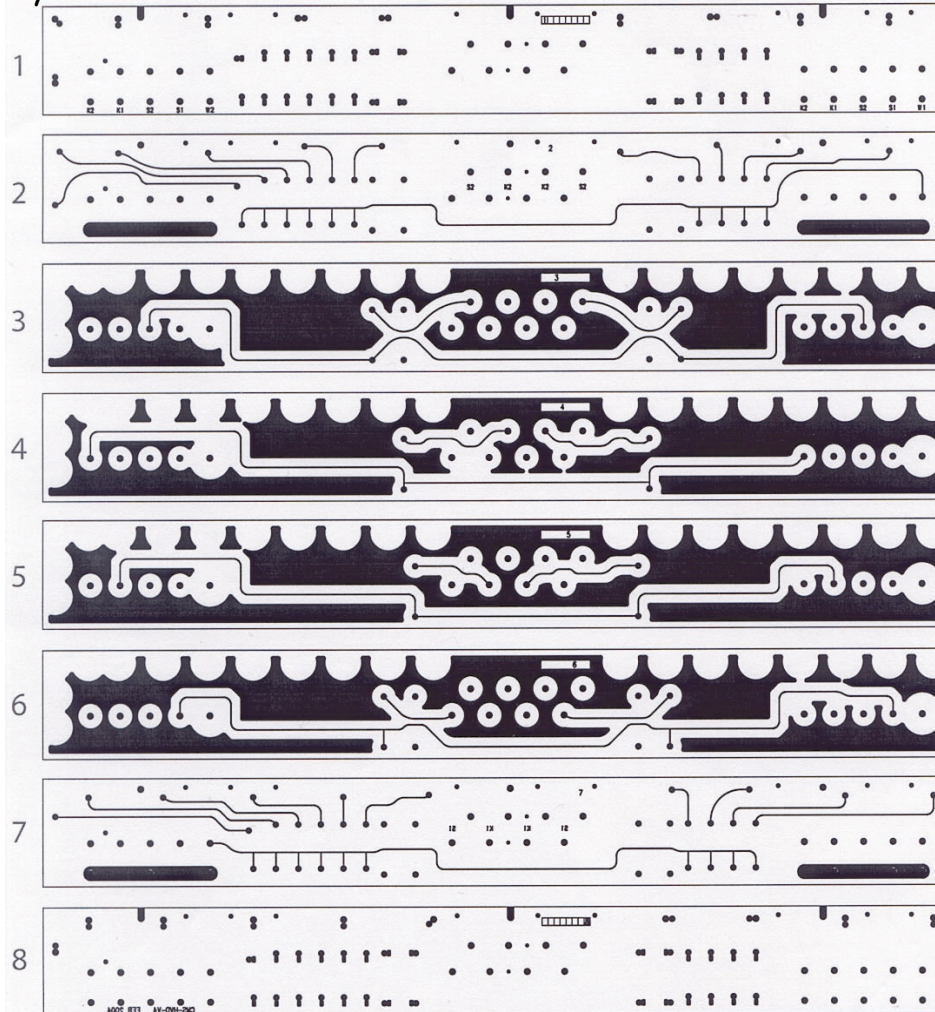
- 1- same inputs and outputs (geometry and labels)
- 2- same number of layers
- 3- ~ 1 mm increase in size; same thickness
- 4- almost no GND in outer layers; GND still in 4 inner layers
- 5- maximized distance between electrodes, in all layers
- 6- rounding: avoided sharp corners at every place
- 7- eliminated unnecessary HV passages through the PCB
- 8- consider using a no-solder layer under the outer prepreg

Thus, with HVB_v4 ("F"),

- 1-3 ensure compatibility with existing chambers
- 4-8 exploit the potential HV safety margins

Overview of all 8 layers of the HVB_v5:

Layer: 040219 P. Zatti + E. Borsato



Pads + components

Wires

Strips

Cathodes

Cathodes

Strips

Wires

Pads + components

HVB_v5:

Layers 2-7 same as for HVB_v4; both ensure max. spacing and >1.5 mm/kV.

- Layers for wires now as inner layers, for safer prepreg adhesion.

- On outer layers have only pads and components (max. spacing).

- HV protection on outer layers: mainly by glue (safer than prepreg "no flow").

- Some minor tuning in progress.

- No cost increase w.r.t. HVB_v4, producer claims (offer).

- THIS VERSION CHOSEN FOR FUTURE at recent DTIC meeting.

From HVB_v1 to HVB_v5:

Optimization of layout:

- Enlarge min. spacing from 0.45 to 1.5 mm/kV, in all layers and also along borders.
- Improve HV insulator on outer surfaces.
- Avoid sharp corners on tracks and pads.
- Minor iteration in progress.
- Ready to contact firms (taking place).

Open issues:

- HV test (insufficient validation of good HVBs)
- Schedule, funding (of course).