III. Physikalisches Institut A

RWTH AACHEN UNIVERSITY

High-rate tests of CMS On-Board Drift Tube electronics

Master's Thesis
Submitted to the III.
Physikalisches Institut A
Prof. Thomas Hebbeker
Physics Department
RWTH Aachen University

by
Matej Repík

Thesis advisor:
Prof. Thomas Hebbeker

Second examiner:
Prof. Oliver Pooth

Registration date: 1.7. 2023
Submission date: 9.1. 2024

Contents

List of Figures

List of Tables

Abstract

As the manufacturing of the Compact Muon Solenoid Phase 2 upgrade hardware approaches, it is crucial to evaluate the developed hardware against the upgrade requirements. A key upgrade part is the improvement of the drift tube system, which requires exchanging the read-out electronics. The new electronics, called On-Board Drift Tube electronics (OBDT), are designed to operate under the conditions of High-Luminosity Large Hadron Collider. This design goal foresees that On-Board Drift Tube electronics cope with 50 Hz/cm^2 hit rate and facilitate precise calibration of their time-to-digital converter using a test pulse system.

This thesis explored inefficiencies of OBDT phi. The measurements present transmission efficiency drop of the experimental setup with background hit rate at 28 Hz/cm^2. The measurements of OBDT theta display efficiency nearly indistinguishable from 100%

Additionally, the irradiation tests of OBDT theta demonstrate that the electronics withstand 70 times the High-Luminosity Large Hadron Collider 0.5 Gy dose. OBDT theta worked continuously during the irradiation, exhibiting little aging effects.

Finally, examinations of time stamp jitter from both measurements describes 1.37 ± 0.33 ns jitter for OBDT phi and 0.32 ± 0.13 ns for OBDT theta.

Acknowledgements

This thesis was performed at III. Physikalische Institut A under the supervision of Prof. Hebbeker, Dr. Eliseev, and Dr. Merschmeyer. It terminates my work at RWTH Aachen University and marks an important milestone. This journey would not be possible without the support I received along this journey.
My first thanks goes to Prof. Hebbeker for allowing me to work at the cutting edge research done in the CMS collaboration. I appreciate the support and encouragement to advance my professional life.
Next I want to say thank you to my advisor Dr. Eliseev who supported and guided me throughout my thesis. I am aware and grateful for the amount of knowledge and experience I acquired while working together. I appreciate the effort and thought Dr. Eliseev put into our discussions and into his feedback throughout my entire work. Finally I appreciate his review of my thesis drafts very much.
Another thanks has to go to Dr. Merchmeyer for his effective and friendly comments, visits at the end of a work day, or responses to my requests for help. I am also very thankful for his review of my thesis drafts.
I also want and have to thank Carsten Presser for hist masterful and yet very social conversations. He was a source of inspiration and a model in many ways. My gratitude also extends for his review of my thesis and his work on the irradiation measurements at CHARM.
Special thanks goes to members of the DT group. I am grateful to Dr. Bellato and Dr. Bergnoli for allowing me to take and helping me with measurements for my master thesis. I also have to thank colleagues from CIEMAT for answering my questions, providing data from and doing the at CHARM, and giving me valuable feedback about my data analysis.
I would also like to thank my institute colleagues for refreshing and recharging encounters in and around work life, be it words of encouragement or simple small talk.
My gratitude also goes to my family and friends for their support, encouragement during my studies. Special thanks goes to Karl Leuckefeld for his feedback to my thesis, the numerous flatmates I had during my thesis work, and Inga Klingebiel for her mental and emotional support during the final writing stages of the thesis.

Chapter 1

Introduction

Particle physics, a vital field in contemporary physics research, seeks to answer one of the most fundamental questions: "What is the universe composed of?" The prevailing theory, the Standard Model, succeeds in this quest by describing the world building blocks as particles. Verifying the theory has been at the forefront of particle physics since its conception in the 1960s [1]. Tests of the Standard Model require complex experimental setups facilitated by particle colliders. The particle colliders also allow research on Standard Model extensions that solve its limitations, particularly, describing dark matter and gravity.

At the heart of Standard Model research is the Large Hadron Collider at Conseil Européen pour la Recherche Nucléaire (the European Organization for Nuclear Research). The LHC, the world's largest accelerator measuring 26.7 km in length, rests about 100 m underground near Geneva [2]. This synchrotron accelerates protons to 6.8 TeV center of mass energy and collides them in four regions, each equipped with sophisticated particle detectors [3].

One such detector, the Compact Muon Solenoid, plays an essential role in observing the collision products. Focusing on one of the many subsystems of the Compact Muon Solenoid, the muon system measures the momenta of muons, practically heavier electrons. The muons form an crucial part of the detector trigger system, and their significance earned them a place in the name of the detector.

To satisfy the increasing demands of Standard Model research, Large Hadron Collider will undergo a High-Luminosity upgrade expected to substantially increase collision rates and data flow. The original design of Compact Muon Solenoid did not plan for the expected luminosity, so the detector requires enhancements. These enhancements are summed up in the Phase 2 Upgrade of the Compact Muon Solenoid.

Situated in the outer layers of Compact Muon Solenoid, the muon system will undergo a significant electronics upgrade. Focusing on the drift tubes, which track the pseudo rapidities up to 1.3, this tracking system will receive new On-Board Drift Tube electronics. The upgrades aim to handle a 7.5-times increase in trigger and muon rates to 750 kHz and 50 Hz/cm^2 respectively [4].

Central to the final development steps of On-Board Drift Tube electronics are tests at the electronics working point. The main requirements include proving

nearly flawless operation under irradiation and constant detection efficiency under increased rates.
This thesis focuses on using the testing system to find out the transmission limits of the On-Board Drift Tube electronics. After the introductory chapter 1, chapter 2 presents essential theories and concepts underpinning particle detectors, starting with the Standard model. Next, the thesis gives an overview of key high-energy physics experiments before explaining the Compact Muon Solenoid and its Muon System. The following chapter 3 shares the background on Phase 2 Upgrade of the Compact Muon Solenoid drift tube system. Explaining the On-Board Drift Tube electronics, chapter 3 also touches on field programmable gate array and time digitization design used in On-Board Drift Tube electronics. Later sections touch on the research this thesis builds upon. Chapter 4 explains testing methods and testing setups of On-Board Drift Tube electronics. The subsequent chapter, chapter 5, presents the test results. The results encompass the jitter of the test pulse system, stability of the time-to-digital converter, and detection efficiency. The thesis concludes with chapter 6 by summarizing the most important findings and proposes the next steps to guarantee successful performance of the Compact Muon Solenoid drift tube system during High-Luminosity Large Hadron Collider operations.

Chapter 2

Particle physics research

People always tried to explain what the world is made out of. The following paragraphs describe the composition of matter characterized by latest scientific theory. After a brief explanation of the Standard Model, the next section presents the Bethe-Bloch formula and bremsstrahlung–a physical theory explaining the processes used to detect some of the charged Standard Model particles. The same section informs on how gas particle detectors use this physical theory and how the Bethe-Bloch formula and bremsstrahlung influence the design of particle gas detectors. The consecutive section gives an overview of the high energy physics experiments at Conseil Européen pour la Recherche Nucléaire (CERN). The final section provides a comprehensive overview of the Compact Muon Solenoid, a general-purpose detector, and delves into the specifics of its Muon System. Additionally, this section offers a detailed explanation of the drift tube chambers.

2.1 The Standard Model

As the most advanced physics theory that describes matter and three fundamental forces of nature, the Standard Model successfully predicts phenomena to an astounding degree of precision. The outstanding achievements of the theory manifest themselves, for example, in predicting the magnetic moment of the electron. As a collection of quantum field theories the Standard Model describes the world using eighteen particles (see Figure 2.1) and 26 parameters [6].

Comparing the state-of-the-art measurement of the anomalous magnetic moment of the electron with its prediction leads to a relative deviation of only $1 \cdot 10^{-9}$ [5].

The theory categorizes fermions, or matter particles, into two groups: quarks and leptons. They are shown in the three left-most columns of the Standard Model diagram (Figure 2.1). The grouping of the particles into three columns represents their three mass generations increasing from left to right. Quarks, in the two upper rows (u, s, t) and (d, c, b), always form heavier composite particles called hadrons or mesons. They do not exist alone. The quark con-

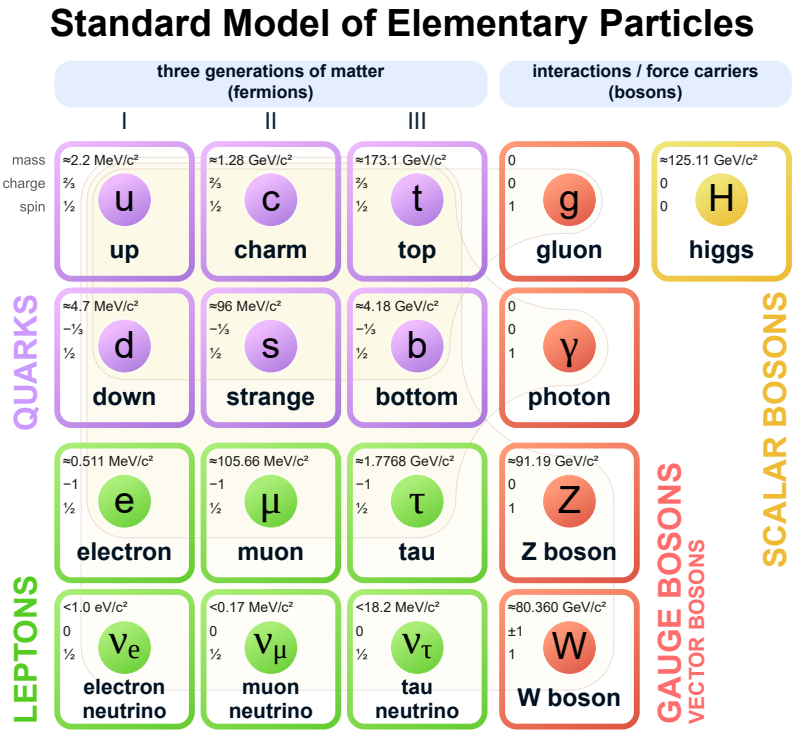

Figure 2.1: A diagram that describes all known matter and force particles plus the Higgs boson. Each square of the diagram includes the particle properties of mass, charge, and spin [7].

finement arises because quarks participate in the strong interaction because it carries color charge. Additionally, all quarks carry fractions of elementary charge e. The top row (u, c, t) carries two-thirds and the bottom row (d, s, b) negative one-third of e. The u,c, and t letters stand for the up, charm, and top quarks; and the d, s, and b letters stand for the down, strange, and bottom quarks. Leptons, however, are detectable by themselves and interact mainly electromagnetically. They are described in the two bottom rows by (e, μ, τ) and $(\nu_e, \nu_\mu, \nu_\tau)$. Only leptons with elementary charge take part in the electromagnetic interaction. Usually, they bond with hadrons of opposite charge and form atoms. If leptons do not have a charge, they interact only through weak interaction and carry the name neutrinos.

The Standard Model also describes bosons or mainly force particles depicted in the fourth and fifth column of Figure 2.1. Photon interacts with charged particles without having charge itself. Also lacking mass, it travels at the speed of light and gives electromagnetic interaction its infinite reach. The gluon facilitates strong interactions and is similarly massless as the photon. Opposite to the photon, it interacts with itself by carrying a color charge. This self-interaction constrains the reach of the strong interaction to the femtometer range. Next, the W and Z bosons represent the force particles of the weak interaction. Unlike the photon and gluon, they have mass and charge. The

bosons allow flavor transformations between the rows of Figure 2.1. Finally, the Higgs boson is the consequence of a Higgs field excitation. As part of the Higgs mechanism, the Higgs field gives masses to most of the particles of the Standard Model, closing an essential gap in the theory [6].
Although the Standard Model describes a significant portion of nature, it has substantial downfalls when stretched to describe gravity and phenomena from cosmology. As of this date, there does not exist a proven and experimentally verified quantum field theory of gravity. Next, dark matter, which forms almost 25% of the universe, does not have particle candidates in the Standard Model. Consequently, the research continues to explore beyond the Standard Model, seeking theories that unify all forces and introduce fermion-boson symmetry (supersymmetry) [6].

2.2 Detecting particles using gas mixtures

When charged particles fly through materials, they lose energy thanks to the interactions they experience. The type of interaction changes based on the material and the particle energy. Interactions relevant to this thesis are ionization, medium excitation, and bremsstrahlung. The Bethe-Bloch formula (equation 2.1) describes the particle energy loss from material ionization and excitation. The process happens when charged particles with high momenta traverse media.

$$-\left\langle \frac{dE}{dx} \right\rangle \approx K\frac{Z}{A}\rho\frac{z^2}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_e\beta^2\gamma^2E_{max}}{I^2}-\beta^2\right] \tag{2.1}$$

where $K = 4\pi N_A r_e^2 m_e \approx 0.307\,\mathrm{MeV\,cm^2/mol}$ is a constant that combines the Avogadro's number N_A, the classical radius of an electron r_e, and electron's mass m_e. β describes the particle rapidity, γ the gamma factor, z the charge, E_{max} the maximum energy. Z describes the atomic number, A the atomic mass, ρ the density, and I the mean excitation energy of the material.
When charged, high momenta particles traverse matter, they ionize a portion of the atoms they interact with, so in gases, the highly energetic charged particles create electron-ion pairs that freely drift until they recombine or interact. Pair creation generates electromagnetic waves. The waves then travel through the medium and generate voltage differences, which can be digitized. The recombination of electrons and ions then produces photons that create unwanted noise. Therefore, the detectors often use a mix of a detection and quenching gas capable of absorbing the generated photons.
Bremsstrahlung becomes relevant when particles have energies high enough to penetrate the electron orbitals of atoms. They interact with the atomic nucleus. The ratio of the particle energy and a square of its mass E/m^2 govern the process. Therefore, highly relativistic particles lose most of their energy because of bremsstrahlung. The electromagnetic interaction with a partially shielded atomic nucleus makes the material traversing particles radiate highly energetic photons. This mechanism creates an energy loss dependent on the

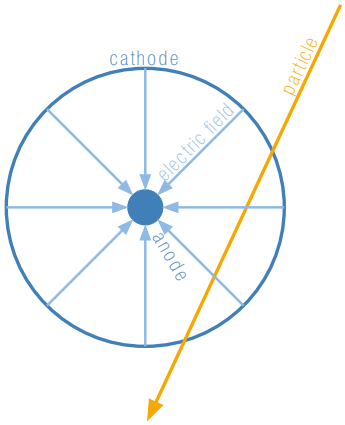

Figure 2.2: A picture of a simple particle gas detector commonly known a drift tube. Its parts include a wire anode, wall cathode, and gas volume in between. When particles pass through, they can interact with the gas and produce detectable signal.

particle energy E and distance traversed x (equation 2.2)

$$\frac{dE}{dx} = -\frac{E}{X_0} \tag{2.2}$$

where X_0 is the radiation length–a material constant characterizing energy loss due to bremsstrahlung. The solution of the differential equation (2.2) comes in the form of an exponential function shown in equation (2.3)

$$E(x) = E_0 \exp\left(-\frac{x}{X_0}\right) \tag{2.3}$$

such that E_0 is the initial particle energy. The function E(x), an exponential decay, describes the particle energy as a charged particle traverses the material.

To maximize the signal, the detection gas should have high density ρ and atomic number to mass ratio $\frac{Z}{A}$ in addition to low mean excitation energy I. The requirements then point to elements in the lower parts of the periodic table that can take on gaseous form, leading to the choice of heavy noble gases.

The design of gas detectors has improved significantly compared to their first conception, and the current state-of-the-art experiments use microscopically structured detectors for particle tracking. Focusing on the most common architecture, a drift tube for example,a gas detector includes a wire in the middle of a gas volume (Figure 2.2). A voltage applied between the wire and walls of the gas volume helps with charge separation and introduces a drift of the electron-ion pairs. The voltage also increases the sensitivity of the gas particle detector [8].

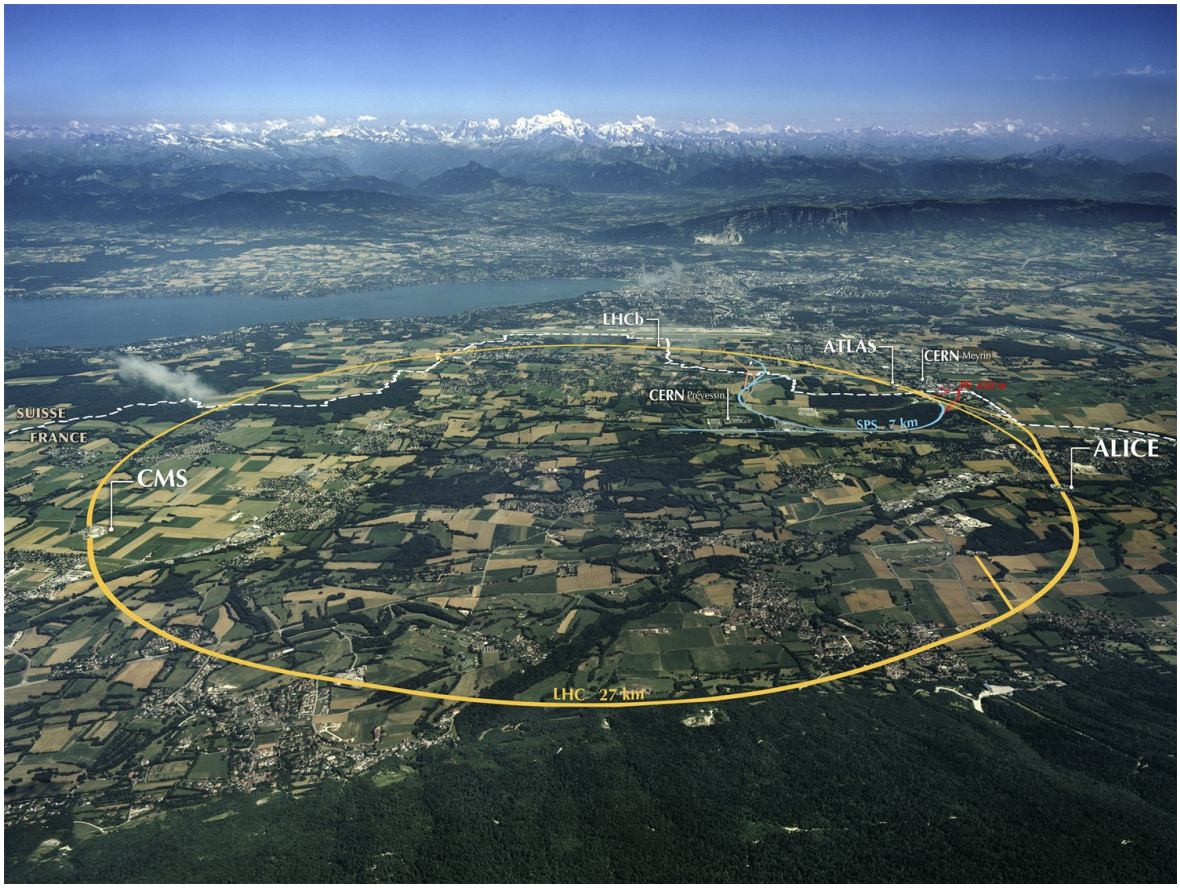

Figure 2.3: The figure presents an areal view of the Large Hadron Collider, showing the location of the four main experiments alongside other CERN sites and pre-accelerators [12].

2.3 High energy particle physics experiments

Probing the standard model and looking for its extensions, the Large Hadron Collider (LHC) accelerates protons and lead ions (Figure 2.3). The synchrotron collides the particle beams at four interaction points around its 26.7 km perimeter. Flying around the collider in bunches, the ions collide at the frequency of 40 MHz during events called bunch crossings. To shield the surroundings from the synchrotron radiation, and collision products, the Large Hadron Collider rests about 100 m underground. Currently, the Large Hadron Collider culminates the accelerator complex at Conseil Européen pour la Recherche Nucléaire (CERN) close to Geneva [2].

The discovery of the Higgs boson in 2012 [9, 10] marks a new chapter for the research at the Large Hadron Collider. The precision measurements and search for Standard Model extensions require increasing the Large Hadron Collider luminosity. An upcoming upgrade, High-Luminosity LHC, aims to significantly raise collision rates by 2029, according to the current plans [11].

Each collision point cavern is equipped with particle detectors to track, measure, and calculate the collision products. Each detector design caters to different research objectives.

- A Large Ion Colider Experiment (ALICE) specializes in heavy ion physics with the largest time projection chamber, tracking the thousands of particles created in the lead ion collisions [13].

- Next, the Large Hadron Colider for beauty (LHCb) focuses on the physics of the bottom quarks and tiny effects of higher order Feynman diagrams in the bottom physics. Compared to other experiments, the LHCb has a conical rather than cylindrical design to analyze collision products close to the beamline [13].

- A Torodial LHC Apparatus (ATLAS), the larger of two general-purpose detectors, uses toroidal magnets for muon bending in its outer layers and utilizes liquid argon electromagnetic calorimeters. It also includes a unique particle identification detector, the transition radiation tracker, capable of tracking particles and distinguishing between electrons and pions [13].

- The second general purpose detector called Compact Muon Solenoid (CMS) has a similar architecture to ATLAS. It has a cylindrical shape composed of the cylinder walls, the barrel regions, and circular cylinder caps, the endcap regions. To eliminate systematic uncertainties, Compact Muon Solenoid uses different detector technologies and designs [13].

The last two detectors are not specialized for any task but utilize different architectures to verify their results. Together, all four detectors enable the Large Hadron Collider to probe the frontiers of particle physics, contributing significantly to our understanding of the universe's most fundamental constituents and forces.

2.4 The Compact Muon Solenoid and its Muon System

The design of Compact Muon Solenoid uses a superconducting solenoid to generate 4 T-strong magnetic field. Its iron return yoke amplifies the residual field to bend muons in the outer layers of the detector. A general overview of the most important parts of the Compact Muon Solenoid can be seen in Figure 2.4.The relative compactness originates from the use of lead tungstate crystals in the electromagnetic calorimeter, the iron yoke, and the 4 T magnetic field. The iron yoke allows placing the muon tracking detectors closer together without sacrificing the lever arm size to guarantee an accurate track curvature measurement.
Keeping the convention of the collaboration this thesis adopts the following coordinate system: the z-axis points along the beamline, the x-axis to the center of the Large Hadron Collider, and the origin rests at the interaction point in the center of the Compact Muon Solenoid [15]. Cylindrical coordinates have a frequent use because of the cylindrical detector structure. Specifically, the radial distance r describes the distance from the beamline, and the z distance

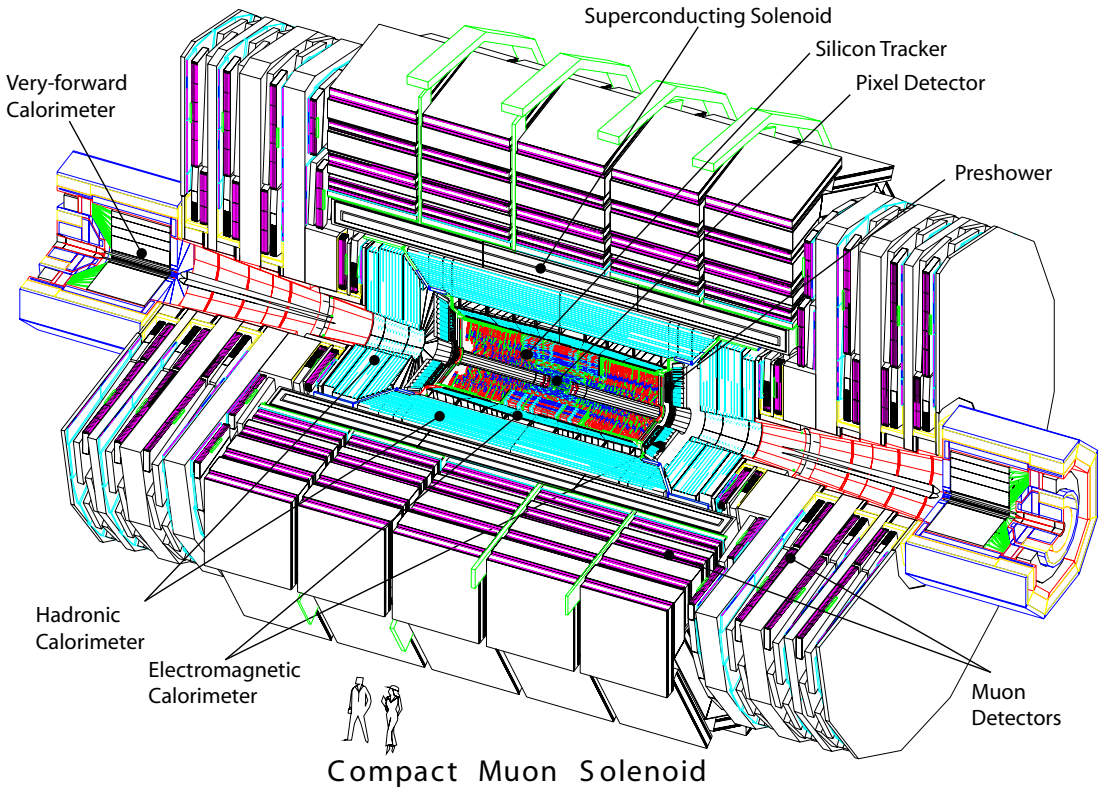

Figure 2.4: A technical drawing to scale showing and describing the Compact Muon Solenoid. The labels describe the most important parts of the detector such as the superconducting solenoid, the electromagnetic calorimeter, and the muon detectors [14].

defines the position along the beamline. The ϕ-coordinate represents the direction perpendicular to the beam line. Finally, the z coordinate is often transformed into pseudorapidity η (2.4), a more natural description for the particle tracks recorded by the detector.

$$\eta = \ln\left(\tan\left(\frac{1}{2}\operatorname{arccot}\left(\frac{z}{r}\right)\right)\right) \tag{2.4}$$

Figure 2.4 illustrates the additional detector systems of the Compact Muon Solenoid. These include silicon tracking detectors close to the interaction point, comprising of Pixel Detector and Silicon Tracker. Next, Compact Muon Solenoid features a pair of calorimeters – the electromagnetic calorimeter (ECAL) and hadronic calorimenter (HCAL) – which absorb the electromagnetic and hadronic showers, respectively. Furthemore, the Muon System, a set of large-area gas detectors is incorporated into the CMS iron return yoke.

- Starting from the interaction point, the first detector encountered by the flying particles is the Pixel Detector. In its current version, its barrel section has four layers. Each of its two endcaps includes three wheels. The silicon pixel sensors have a pixel size of 100×150 —m^2 allowing the

resolution of 10 —m in the r−ϕ dimensions and 20 —m in the z direction [15].

- Afterwards, the particles traverse the Silicon Tracker. The sub-detector modules use a more economic simplification of silicon pixels called microstrips with dimensions of $10^5 \times 80$ —m^2 and $2.5 \cdot 10^5 \times 180$ —m^2. The granularity of the silicon sensors decreases with the increasing distance from the beam pipe, allowing for construction of 200 m^2-silicon based sub-detector [15].

- The next detector system starting beyond 110 cm away from the beam line comprises 68523 lead tungstate ($PbWO_4$) scintillators. They form the electromagnetic calorimeter and absorb the photons and electrons generated by the collisions. In conjunction with avalanche photodiodes (barrel section) and vacuum phototriodes (endcap section), they allow measuring the energy of absorbed particles [15].

- Hadronic particles are absorbed in the hadronic calorimenter built with brass and plastic scintillator sandwich calorimeters. Light-shifting fibers incorporated in the plastic scintillators maximize light collection and protect readout electronics. The light digitization happens with silicon photomultiplies [16].

- The finally detection system for the residual particles (99% muons) is the Muon System [4]. Composed of barrel and endcap sections, it tracks particles over large areas using gas detectors. The endcaps cover pseudorapidities $1.3 \leq \eta \leq 2.4$ and use Cathode-Strip Chambers (CSCs) for tracking. A Cathode-Strip Chamber is a thin multi-wire proportional chamber with segmented strip readout for enhanced precision. Meanwhile, the barrel region uses drift tubes and tracks particles up to $\eta \leq 1.3$. Both endcaps and the barrel utilize Resistive Plate Chambers (RPCs) to capitalize on their excellent 3 ns timing resolution [15]. The Resistive Plate Chambers employ two gas layers, each 2 mm thin, with readout strips between these volumes to collect the signal.

Barrel regions of the CMS Muon System are covered by four layers of drift tube muon chambers (Figure 2.5) and four layers of Resistive Plate Chambers. Both detector types track muons, and the drift tube muon chambers reach accuracy of 100 —m. The lower numbers in the naming scheme of the Muon chamber Barell (MB)–MB1, MB2, MB3, or MB4– indicate the proximity of the chamber to the interaction point. The MB1 to MB3 chambers include three super layers. One super layer measures the z-coordinate of the CMS detector, and the other two measure the ϕ-coordinate. MB4 chambers only incorporate two super layers measuring the ϕ-position. Each DT muon chamber can measure ther-coordinate of a track, owing to the precisely known position of the chambers. Super layers combine four layers of drift tubes in a staggered configuration. The arrangement showed in the left part of Figure 2.6 resolves the directional ambiguity of a single drift tube [4].

Figure 2.5: A picture of an MB1 chamber in the III. Physics Institute A at RWTH Aachen University. The vertical gap between the blue connectors serves as a storage for the Minicrate.

The CMS drift tube (DT) is engineered in order to create a nearly constant drift speed for the electron-ion pairs (Figure 2.6 left). Simulations of the arrangement of the gold-plated tungsten wire and aluminium anodes and aluminium cathodes show a nearly constant electric field that guarantees the nearly constant drift velocity v_d = 54.3 —m/ns. Shaping the electric field involves setting the tungsten wire at 3600 V, the alumnium anode at 1200 V, and the aluminium cathode at –1800 V. In the 13 mm×42 mm drift tube flows a mixture of 85% argon, detection gas, and 15% carbon dioxide (CO_2), quenching gas, at a slight over-pressure of 30 mbar compared to the atmosphere [17, 18].
Shaping and discriminating the signals from the wires, the font-end electronics forward the voltage drops arising from particle hits. Also known as front-end boards (Figure 2.7), their main functionality manifests in the Multichannel Amplifier-Discriminator (MAD) application-specific integrated circuit (ASIC) [20, 4]. Four of MAD chips are soldered on a front-end board, processing 16 channels. Consequently, each MAD is capable of amplifying and discriminating signals from four drift tubes. Apart from signal processing the front-end board includes slow control communication and test pulse lines. The slow control allows channel masking and temperature monitoring both implemented in the MAD ASIC [20, 21].

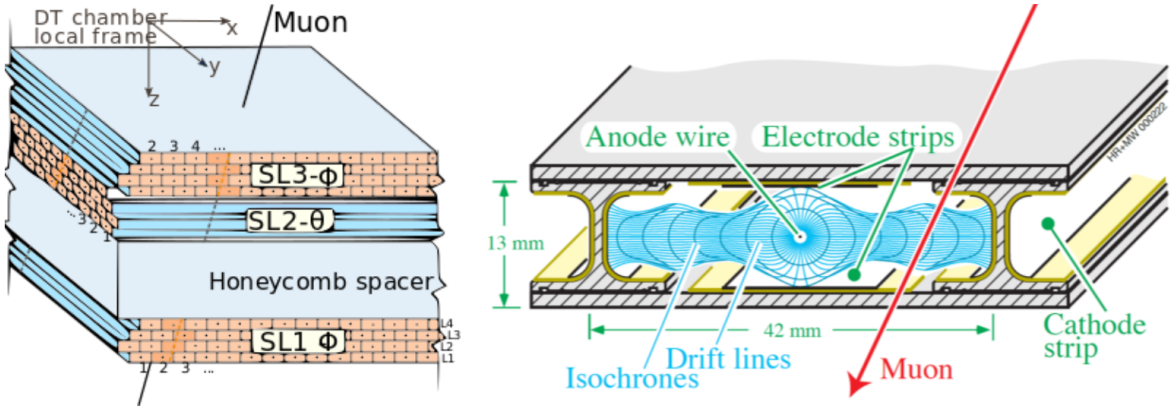

Figure 2.6: A drawing that describes the arrangement of drift tubes in a three super layer chamber. The SL acronyms describe the super layers and L stands for layer. The right diagram shows the drift tube design used in the Compact Muon Solenoid. The long turquoise drift lines in the diagram depict the electric field. The lines perpendicular to them are equipotential lines or isochrones [19].

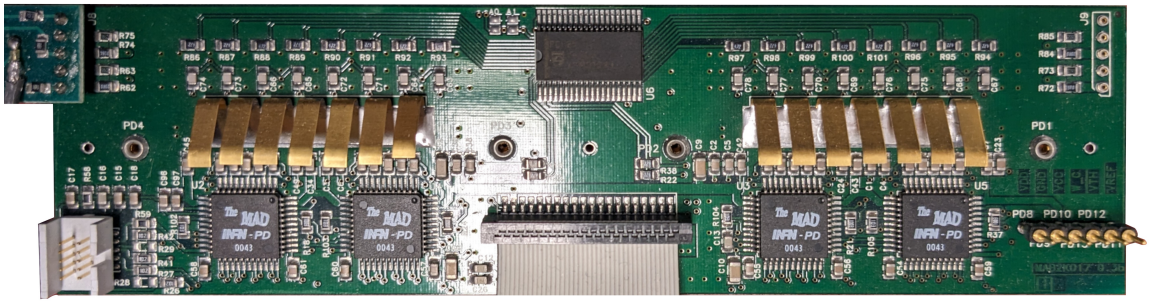

Figure 2.7: Figure shows the front-end board in a close up. Four MAD chips are soldered close to the bottom edge of the front-end electronics.

The test pulses couple to drift tube lines and trigger 32 channels at a time. Because of the relatively long electron drift times the drift tube chambers need to have precise timing information. To calibrate the required time to digital converters the front-end boards uses test pulses. They arrive the front-end boards simultaneously and allow to subtract the signal path differences naturally arising different cable and trace lengths.

The final part of the present Muon System are the read-out electronics. They are composed of a few systems integrated together in a metal casing screwed to one side of the muon chamber. Minicrate, as the casing is called, houses read-out board (ROB) and trigger board (TRB) responsible for data acquisition and triggering respectively. Electronics for the muon chamber slow control and communication are also included in the Minicrates.

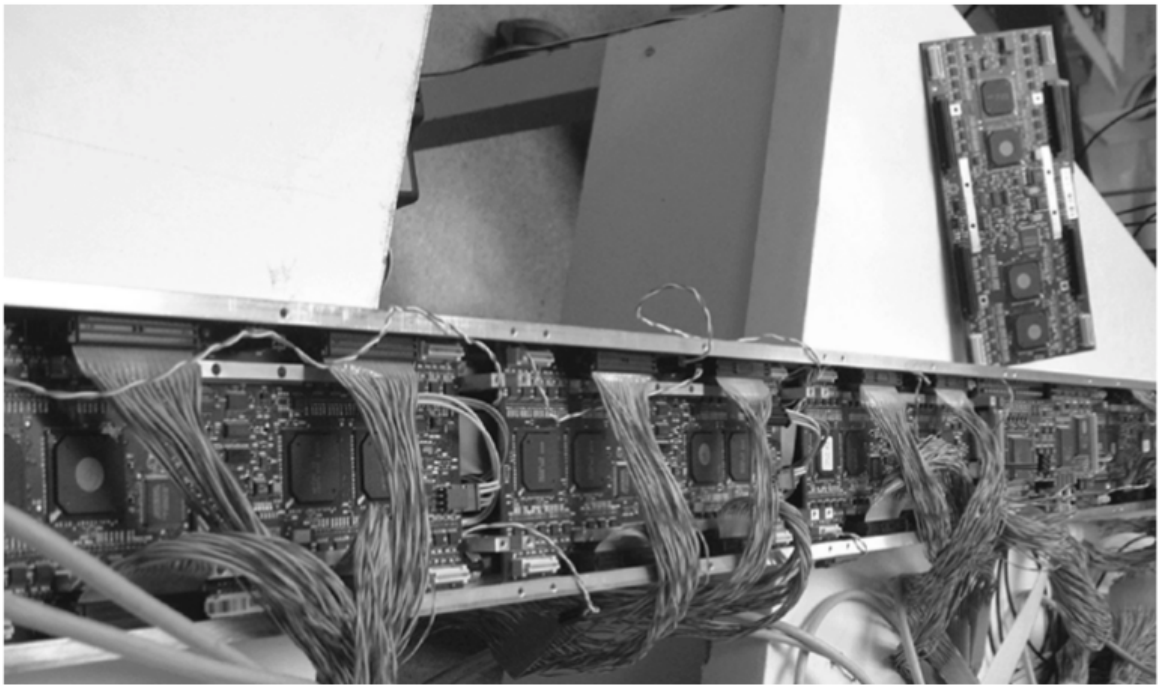

Figure 2.8: A picture of the legacy minicrate together with the read-out board [17].

Chapter 3

Upgrade of the CMS Muon System

Advancing from the general overview in the previous chapter, this chapter focuses further on the imminent upgrades of the Compact Muon Solenoid Muon System. The chapter begins by detailing the On-Board Drift Tube electronics – the new read-out electronics to be installed onto the muon chambers. Given the use of field programmable gate arrays in the On-Board Drift Tube electronics, the chapter describes their most important operational principles. Subsequently, the process time digitization within the field programmable gate array (FPGA) firmware will be explored. Transitioning to summary of crucial findings from existing research, the chapter lays the research foundation this thesis builds upon.

The consequences of the High-Luminosity LHC require improving all CMS sub-detectors. Collectively the changes are aggregated in the Phase 2 Upgrade. The detector irradiation tests and simulations show manageable radiation degradation of drift tubes [4]. Therefore, only the readout electronics of the muon chambers need exchanging. The reasons for the interchange are the following:

- increase of level-one trigger rate to 750 kHz from 100 kHz,
- insufficient radiation hardness of the current electronics,
- muon chamber trigger generation across chambers.

Moreover, the existing stockpile of current electronics is insufficient to provide enough replacements for the entire operation of High-Luminosity LHC [4]. Although the new electronics only expect an estimated dose of 0.5 Gy, the failure rate of the old electronics under these conditions exceeds the available replacements [22]. To easily compare old and new components, the DT group adopted a naming scheme of "legacy" that describes the original hardware and electronics.

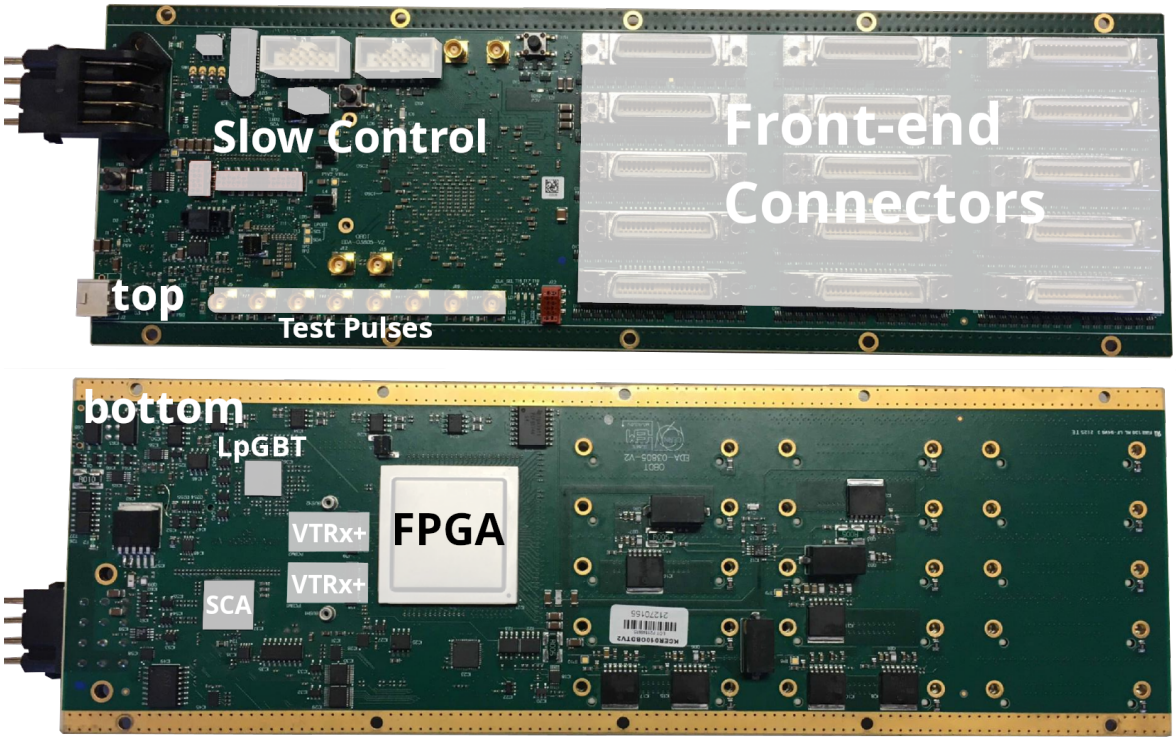

Figure 3.1: A Figure that shows the front and back side of the OBDT phi. The most important components of OBDT phi are highlighted in white.

3.1 On-Board Drift Tube electronics

The main purpose of On-Board Drift Tube electronics (OBDT) is to time stamp and give spatial coordinates to the signals coming from the front-end boards (Figure 3.1). On top of locating particle hits in time and space, the readout electronics also transfer the data to the backend electronics. The presence of timing digitization also necessitates a calibration of the systematic time offsets. This task is taken care of by the test pulse system controlled by On-Board Drift Tube electronics. The test pulses are sent at the same time and propagate through the muon chamber front-end electronics. They feed into the lines coming from the drift tubes and elicit a hit response from the MAD chips. This response then reaches On-Board Drift Tube electronics. One test pulse activates eight front-end board channels simultaneously [21].
Because many legacy systems are present, the new readout electronics also have to communicate with and control the systems. As a consequence, On-Board Drift Tube electronics handles slow control of the muon chamber front-end boards (FEBs). The On-Board Drift Tube electronics can mask noisy channels and monitor the temperature sensors implemented in the Multichannel Amplifier-Discriminator chips. Forwarding the monitored chamber pressure is also part of On-Board Drift Tube electronics design. Finally, the On-Board Drift Tube electronics are capable of monitoring their own temperature [23].
The DT group developed two types of read-out electronics. The parts, or super layers, of chambers measuring the ϕ-coordinate of the track running around

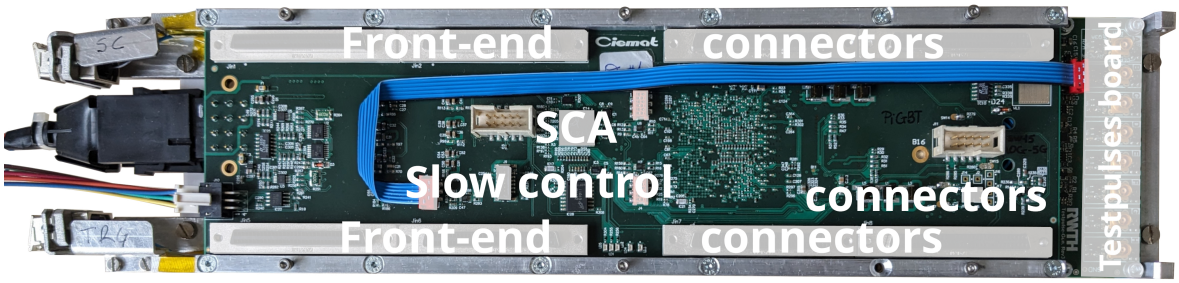

Figure 3.2: A Figure that shows the front of the OBDT theta. The whiter regions of the picture highlight the most important components of On-Board Drift Tube electronics and the Testpulse board.

the beam pipe will be connected to OBDT phi. Covering the angle from the beam pipe θ, the other super layers are read out by OBDT theta. The main reason for this design decision comes from two cabling schemes. The front-end cables connected to the theta super layers cannot be exchanged.

Taking a closer look at the design in Figure 3.1, OBDT phi includes fifteen connectors for the low-voltage differential signal (LVDS) cables on its top side. These cables originate the muon chamber and add up to a total of 240 channels with sixteen channels per connector. On the top side, there are connectors for all the slow control and monitoring services. Additionally, this side also houses eight test pulse connectors, which are used for sending signals to the front-end electronics of the muon chamber. The bottom side, on the other hand, houses most of the integrated circuits (ICs), i.e. the low-power gigabit transciever (lpGBT), slow control adapter (SCA), Versatile Transciever Link plus (VTRx+), and a field programmable gate array (FPGA) [24, 25, 26, 27].

The second, theta, version of On-Board Drift Tube electronics differs from the phi in its connectors and test-pulse system. Closely resembling the legacy read-out boards (ROBs), the design of OBDT theta has to cope with using the legacy front-end cables. As a consequence, the front-end cable adapters rest on the borders of the board. The top side also includes connectors for slow control and control of the test pulse system, slow control adapter, and memory (Figure 3.2). Similarly to OBDT phi, the theta has most of its computational power on the bottom. The Polarfire field programmable gate array, low-power gigabit transciever, and two Versatile Transciever Link plus face the solid aluminium frame [27, 24, 26]. Finally, the test pulse generation is taken over by a separate board, the Testpulse board. Powered and operated by OBDT theta, the Testpulse board simultaneously generates eight signals that propagate to the front-end boards.

The main computational center of On-Board Drift Tube electronics, a field programmable gate array, takes care of the time digitization, data packet formatting, and time-precise test pulse control. The DT group chose Microsemi Polarfire MPF300 field programmable gate array [27]. Taking a closer look at its configuration (Figure 3.3), the signals from the front-end boards go through the time-to-digital converter. Once the voltage transition gets assigned to a

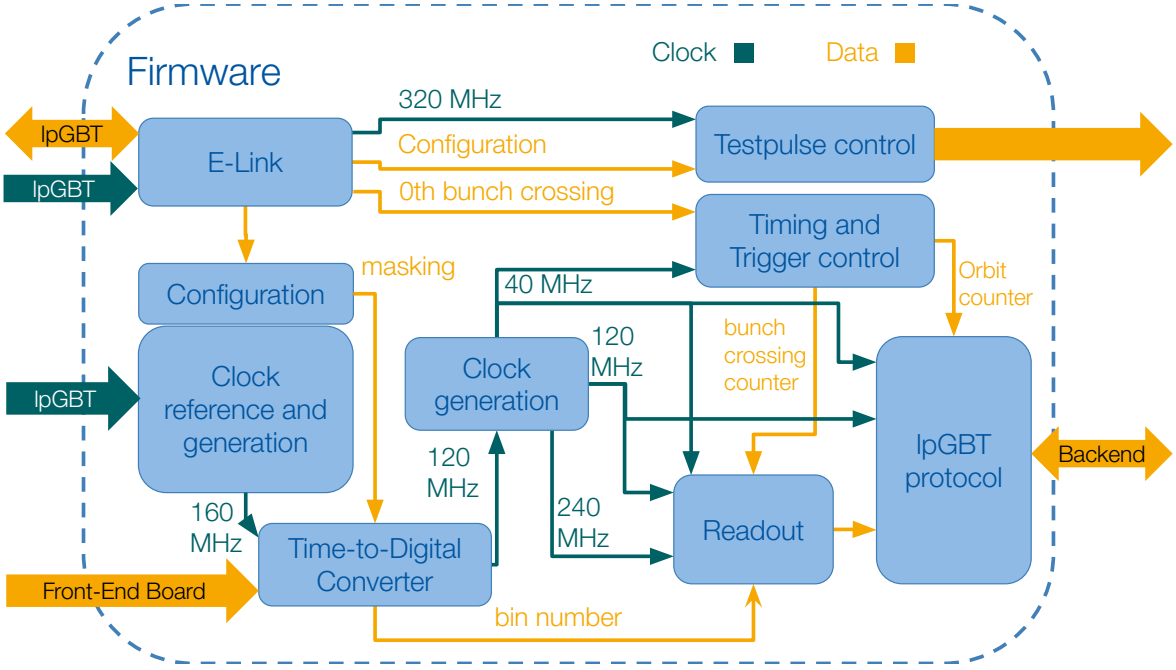

Figure 3.3: A diagram that shows the most important parts of the firmware developed for the On-Board Drift Tube electronics (based on [23]).

bin number, the field programmable gate array packages the time bin, channel number, OBDT number, and the muon chamber number to a packet [23]. Then the packet is sent through the lpGBT protocol to the backend [28]. The FPGA firmware can also mask channels.
The 40 MHz clock reference is reconstructed in the field programmable gate array thanks to packets received by low-power gigabit transciever. Other clocks generated in the field programmable gate array with frequencies three-, four-, six-, eight-, and 16-times higher use the 40 MHz clock as a reference. The clocks find use in the time-to-digital converter, Timing and Trigger control, Readout, Testpulse control, and lpGBT protocol blocks. The highest 641 MHz [23] frequency enables splitting one tick of the reference clock into 32 bins. Thus the timing resolution of the On-Board Drift Tube electronics reaches 0.78 ns.

3.2 Field Programmable Gate Arrays

Shortly described as a technology for re-programmable application-specific integrated circuit, field programmable gate arrays fill today's demand for increasing flexibility and optimization of electronics. An FPGA includes logic gates, storage, look-up tables, processors, multiplexer, demultiplexer, and multiple types of input and output. For example, these building elements allow path length matching the inputs and outputs of the field programmable gate array. The mentioned parts of the electronics allow for parallel signal processing with a fixed processing time. Because the FPGA building block can be con-

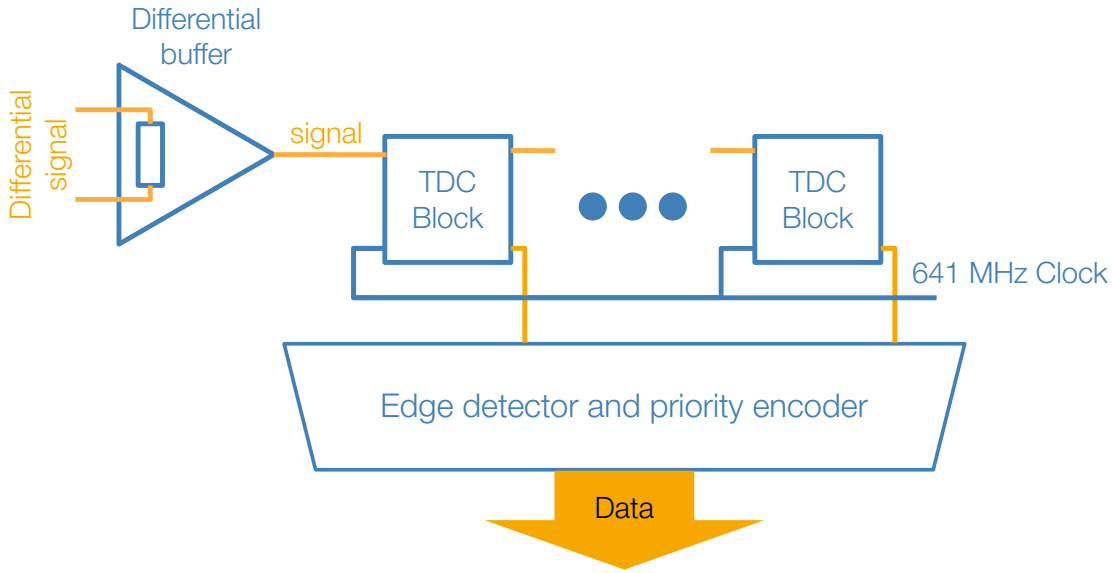

Figure 3.4: A schematic describing the time-to-digital converter (TDC) architecture used in OBDT FPGA. The differential signal passes through a differential buffer and then multiple TDC blocks running at different clock phases (adjusted from [28]).

nected in and re-wired many times over, the field programmable gate arrays allow online rewiring of electronics. This flexibility has an outstanding advantage compared to conventional electronics because it allows fixing design after start of official operations. Additionally if the performance of the set wiring degrades, field programmable gate array can be simply reprogrammed to use its sections that work as expected. Most advanced experiments today utilize field programmable gate arrays because of the limited signal processing times constrained by the time between the particle collisions [8]. Field programmable gate arrays can reach timing resolution of less than 1 ns. Together with their flexibility, robustness, and radiation hardness, they make an essential part of On-Board Drift Tube electronics.

3.3 Time digitization in On-Board Drift Tube electronics

Determining time allows a correct reconstruction of events and thus makes an essential part of the collider experiments. The process involves sampling a signal line and detecting the change in voltage. After the sampling, the bit words are then translated to numbers that describe the bin number in which the voltage transition happened.
Focusing on the implementation in the Polarfire FPGA, the sampling process happens in TDC blocks (Figure 3.4). They include deserializers running under a sampling clock. In the case of On-Board Drift Tube electronics, the sampling

clock runs at 641 MHz. Generated in OBDT's field programmable gate array, the clock is phase aligned to and runs at 16-times the frequency of the 40 MHz LHC clock. To reach the 32-bit resolution the firmware duplicates the 641 MHz clock and phase shifts it by 180°.
Afterward, the deserialized signal from the front-end boards arrives at the edge detector. The edge detector takes in a bit word and determines which of the bit changes represent an edge. In addition to the detection task, it should be robust enough to filter out noise. Finally, once the edge detector determines the transition bin, it forwards its information to the encoder that generates an integer representing the number of the transition bin.
Time deserializers appear mostly in telecommunication devices and work with bit words that include alignment bits. Re-purposing deserializers for time measurement is an ingenious solution with some drawbacks. One drawback is that the rising edge of the signal might coincide with the rising edge of the sampling clock. This coincidence necessitates an accurate characterization of the time-to-digital converter to see the behavior of the first TDC block used in the deserialization chain [28].

3.4 On-Board Drift Tube electronics slice test

Because the development of On-Board Drift Tube electronics reaches later stages, the On-Board Drift Tube electronics has already been successfully tested in the readout chain. Thirteen boards were wired parallel to the current muon chamber read-out electronics, the read-out boards (ROBs) and trigger boards (TRBs), while cosmic muons generated tracks in the muon chambers. Figure 3.5 compares the read-out chains. The use of On-Board Drift Tube electronics significantly simplifies the architecture. Deployed in one barrel sector of the Compact Muon Solenoid, the still ongoing test campaign called slice test covers all types of muon chambers, MB1, MB2, MB3, and MB4. Since the Phase 2 upgrade changes the readout and trigger architecture of the muon chambers, the slice test also proves the new back-end electronics.
The initial outcomes of the slice test are encouraging, especially in the aspect of online track reconstruction. The new read-out electronics have significantly enhanced the timing accuracy of the trigger evident by narrower distribution in Figure 3.6. With On-Board Drift Tube electronics, the trigger primitives – track sections with time stamps – are processed faster. The more swiftly generated trigger primitives lead to more accurate timing information about muons traversing the muon chambers. The increased timing accuracy showcases the design efforts aimed at negating the effects of pileup.
Additionally, the slice test uses each read-out electronics as an efficiency reference for the other. These cross-hit efficiencies show a consistent behavior across both read-out electronics generations (see Figure 3.7). Apart from the masked channels, the rest of the MB3 channels show efficiencies in the green regions of the color map. Upon closer examination, most of the channels reach almost 100%, so the new electronics detect exactly as many hits as the legacy ones.

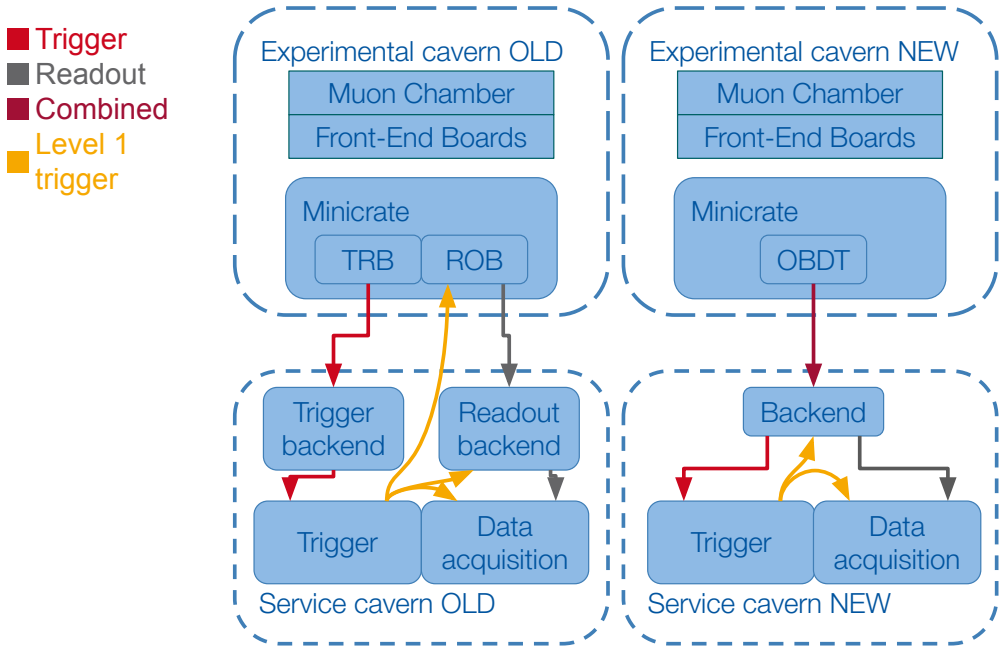

Figure 3.5: A diagram that allows comparing the legacy and new muon chamber readout. The new architecture reduces the amount of on-detector electronics (based on [28]).

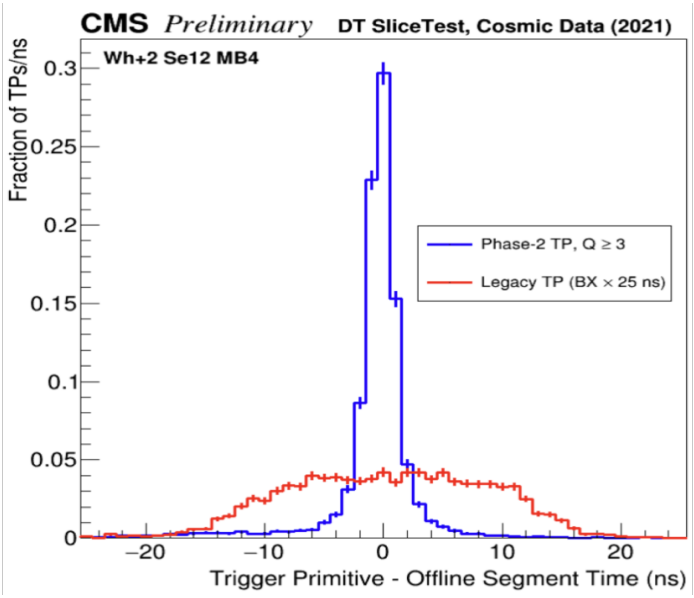

Figure 3.6: A histogram that compares the timing performance of trigger primitives generated with trigger board and On-Board Drift Tube electronics. The red histogram describes the legacy trigger board and the blue histogram the new On-Board Drift Tube electronics [29].

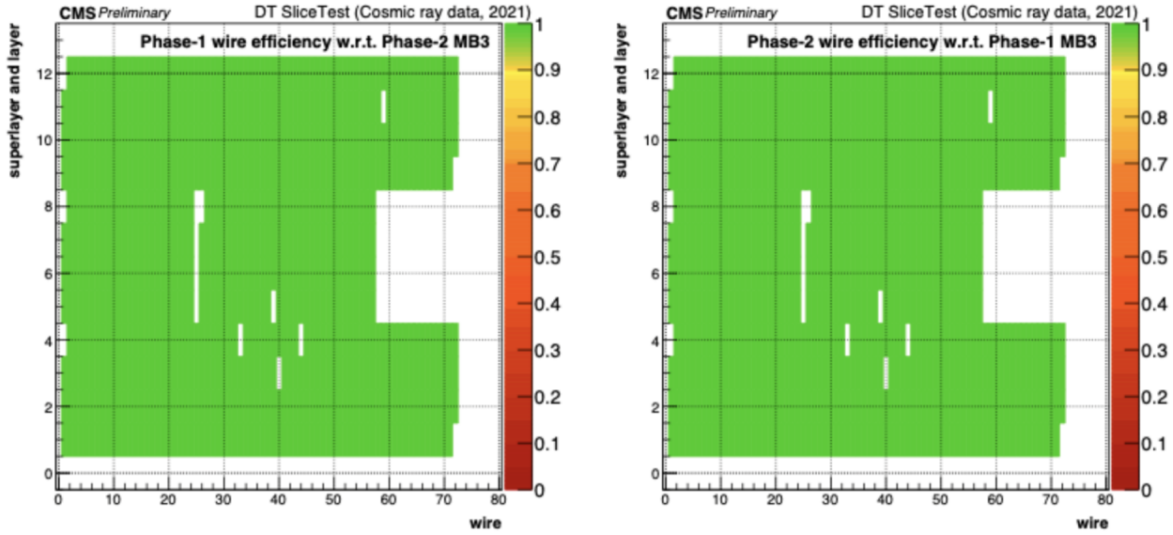

Figure 3.7: A two-dimensional histogram that compares the efficiencies of legacy (left) and new (right) read-out electronics. The x-axis describes the wire number in a drift tube layer, and the y-axis the layer number [29].

3.5 Time digitization tests of On-Board Drift Tube electronics

Because of the possible coincidence of the sampling clock and signal edges mentioned in section 3.3, the DT group already characterized the time digitization capabilities of the OBDT firmware. Because time measurement involves digitization, the group examined the differential non-linearity (DNL). Additionally, they looked at channel cross-talk. The characteristics were measured by injecting a non-correlated random signal to the channels of the field programmable gate array. The cross-talk measurements injected the signal either to both the primary and neighboring channels or to the primary channel only. All tests satisfied the benchmarks set by the DT group.
Differential non-linearity describes a metric that gives a numerical value to how much the width of the time bin deviates from the ideal. A perfect time-to-digital converter splits a time interval into bins with the same width. Because the real world does not allow for perfect precision, the measure of differential non-linearity defined in the equation(3.1)

$$\mathrm{DNL}_i = \frac{t_{i+1} - t_i}{C} - 1 \quad \text{for} \quad i = 1, \ldots, 2^n - 1 \tag{3.1}$$

where DNL_i stands for the differential non-linearity of the i-th bin, t_i the i-th bin boundary in units of time, C a constant for converting time intervals into integers produced by the time-to-digital converter, and n being the number of bits the time-to-digital converter operates with. Combined, differential non-linearity allows to sum up the aforementioned inaccuracy in one number [8].
The tests of differential non-linearity performance show promising results.The measurements show that differential non-linearity stays within the requirement

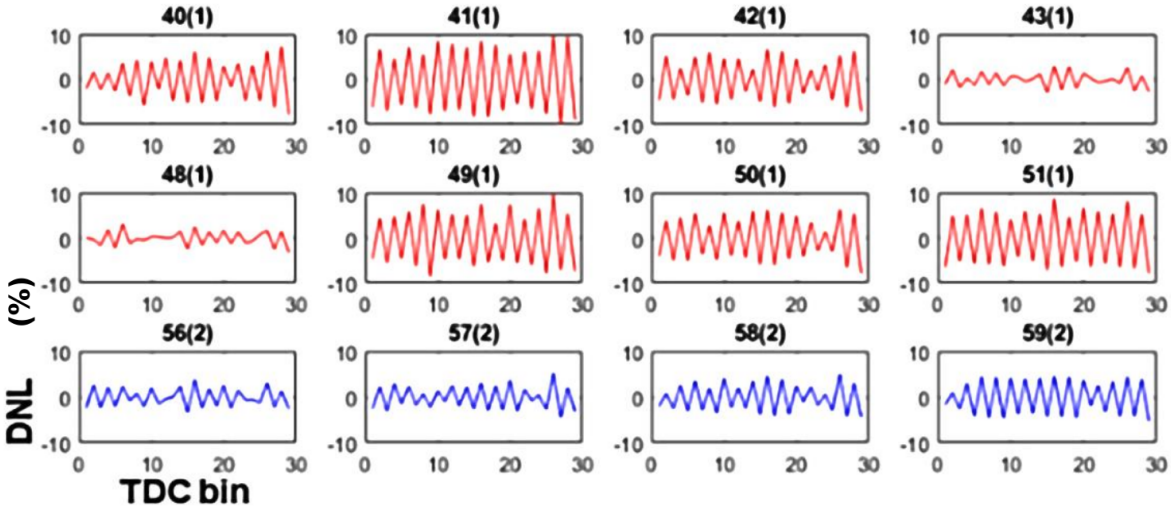

Figure 3.8: A series of plots showing the differential non-linearitys of the time-to-digital converter implemented in the Polarfire field programmable gate array. The twelve distributions the measured data. The distributions of the The x-axis of the plots describes the time bin and the y-axis the differential non-linearity in percentage [23].

±10% (see Figure 3.8) [23]. Differences between channels, for example, channels 41 and 48, mainly come from different clock domains of the field programmable gate array.
Additionally, the tests that examine the influence of neighboring channels on one another show a below 1% effect Figure 3.9. Examining the plot with a time-to-digital converter bin on the x-axis and differential non-linearity in percent on the y-axis, the channel cross-talk for channel 257 shows a visible difference between the red dashed line and the full green line. For most bins, the cross-talk increases the differential non-linearity.
The time digitization tests show that the time-to-digital converter on implemented on On-Board Drift Tube electronics fulfills the set goals. Its differential non-linearity stays within 10%. Next the measurement of cross talk demonstrates a below 1% effect on the differential non-linearity. Both results illustrate low internal jitter and high accuracy of the time-to-digital converter. The data demonstrate readiness of the time digitization system of the On-Board Drift Tube electronics.

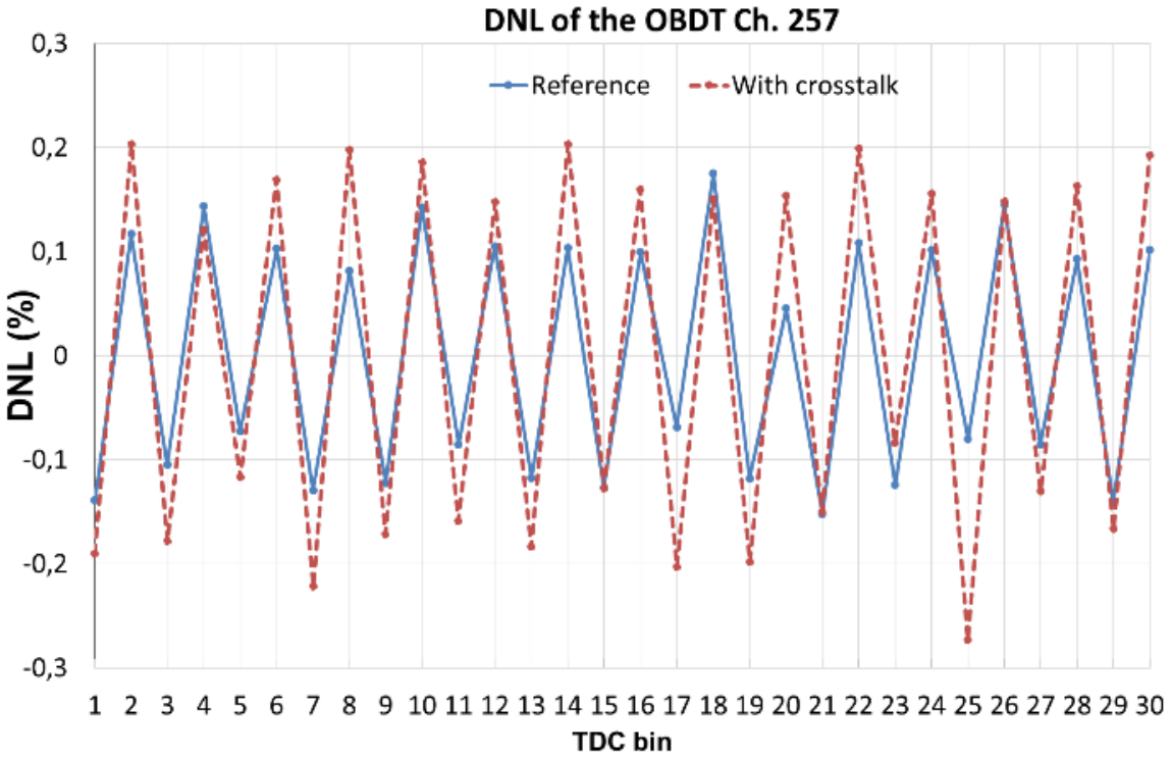

Figure 3.9: An example of a cross-talk influence on a differential non-linearity of an OBDT channel. The x-axis of the plots describes the time bin and the y-axis the differential non-linearity in percentage [23] .

Chapter 4

Setup for On-Board Drift Tube electronics tests

This chapter focuses on describing the testing methods and experimental setups. First, the opening section describes how the test pulse system of the On-Board Drift Tube electronics emulated hits in for the muon chamber front-end electronics. The two measurement campaigns presented in this thesis used slightly different methods for hit emulation, so both of these methods are described in the opening section. The next section introduces the experimental setup used for the measurements on OBDT phi at Istituto Nazionale di Fisica Nucleare Legnaro and the third section introduces the experimental setup used for the measurement on OBDT theta at CERN high energy accelerator mixed field facility.

On-Board Drift Tube electronics have not yet been tested for the expected higher rates. Proving the electronics can handle the High-Luminosity LHC hit rates of 50 Hz/cm^2 is essential for the development process [4]. Therefore, part of the work focused on emulating these rates, presenting an opportunity to examine the test pulse system. The rate of cosmic muons does not reach 50 Hz/cm^2, so the thesis presents creative testing procedures that allow for high-rate tests. Since the testing method does not depend on a test beam, it is a cost-effective solution applicable across the DT Group.

4.1 Emulating hits using the test pulse system

High-rate tests of On-Board Drift Tube electronics executed as part of this thesis rely on the test pulse system. By using the test pulses, the high-rate tests simultaneously examine the On-Board Drift Tube electronics and the test pulse system. As mentioned in 3.1, the test pulse command originates in the FPGA of OBDT. After being generated, they propagate towards the chamber front-end electronics. First the MAD chips recognize test pulses as signals. Then the chips send hit signals to the On-Board Drift Tube electronics. The FPGA

pins that receive a signal from a front-end board are called channels. Numbered 0 through 239, their indices allow differentiating between input signals. A complex mapping scheme allows matching the channels to a drift tube.
Synchronized with the rising edge of the 40 MHz LHC clock, the test pulse system can simulate hits for all 240 channels On-Board Drift Tube electronics can monitor. The test pulses are issued by a single FPGA pin and should be "simultaneous" within one bunch crossing. Multiplying 40 MHz by 240 channels, the test pulse system can theoretically generate 9.6 GHz average hit rate for one On-Board Drift Tube electronics. This rate far exceeds the expected operational rate of 1.7 MHz hit rates for both OBDT types.
The generated average hit rate is further limited by the software[1] used for controlling the test pulse system. This software reduces the maximum hit rate by the limiting of the On-Board Drift Tube electronics command rate to 2.4MHz. The mentioned rate comes from a conservative limit of the measured execution time of a line in Python $\approx \frac{1}{100\,\mu s}$ multiplied by 240, the number of channels On-Board Drift Tube electronics can process.
The core objective of these tests is to determine the transmission limits of On-Board Drift Tube electronics. The testing procedure, developed for this thesis, progressively increases the number of activated channels, sends test pulses, and records the returned data. A precise description of the test follows:

1. Initially, all channels are deactivated.
2. Then one channel is activated.
3. A test pulse is sent and the system waits one second.
4. An additional channel is activated.
5. Subsequently, a test pulse is sent and the system waits.
6. The previous steps are repeated until all 240 channels are active.

Channels are activated by unmasking in two possible fashions. The first method involves using the muon chamber front-end electronics. Controlled by the inter-integrated circuit (I^2C) bus, the front-end electronics receive a control word issued by On-Board Drift Tube electronics and then mask or unmask the addressed channels. The second masking method directly blocks the FPGA inputs within the Polarfire FPGA.
To test the influence of both of these masking methods, the testing software includes the use of FPGA masking first and then the combination of the two.
A simpler version of hit emulation happened during the irradiation test of OBDT theta at CERN high energy accelerator mixed field facility (CHARM) (see section 4.3) [30]. The test pulses were issued without masking and at lower rates of 291 Hz per channel, calculated by issuing 2911 test pulses over 10 seconds. After 10 seconds the testing system recorded data and took a snapshot of the system state.

[1] https : //gitlab.cern.ch/abergnol/obdtv2_backend_firmware

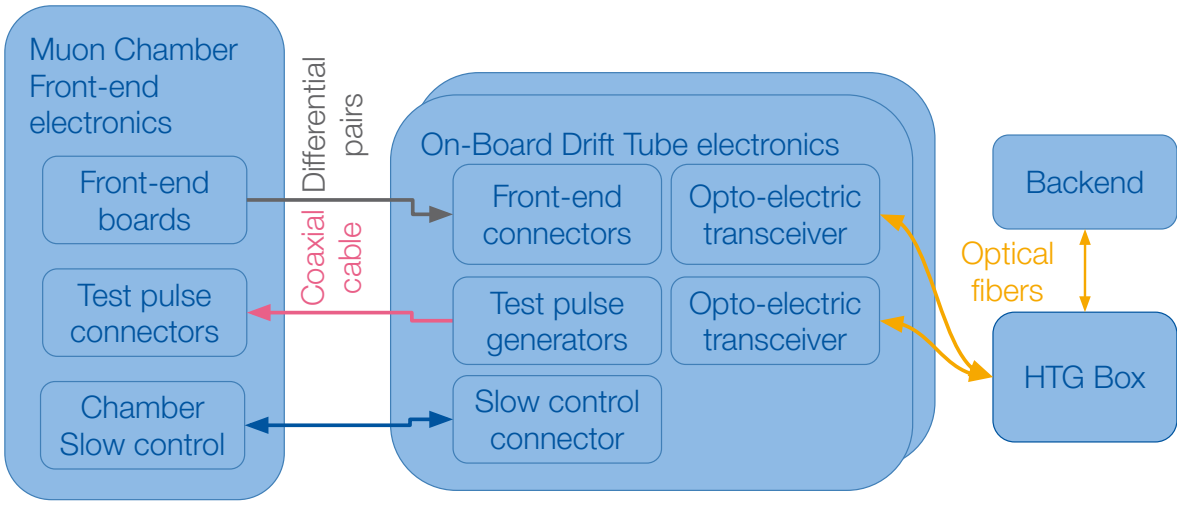

Figure 4.1: A symbolic diagram that describes the experimental setup for OBDT phi tests.

Two variants of test pulses were issued in the CERN high energy accelerator mixed field facility. One type propagates through the muon chamber front-end electronics. The source of this test pulse signal changed every minute thanks to the multiplexer. The other test pulses originated at the OBDT theta front-end connectors and looped back to another front-end connector. These tests ensure the radiation hardness of the On-Board Drift Tube electronics and the Testpulse board. Online monitoring of the tests recorded time stamp histograms, the number of missing hits, and other less relevant monitoring data such as temperatures, humidity, OBDT input power, etc.

4.2 Hardware used for testing OBDT phi

The high-rate test of OBDT phi was conducted at Istituto Nazionale di Fisica Nucleare (INFN) Legnaro as part of this thesis. Using the local experimental hardware, the tests included only the muon chamber front-end board. Given the history of INFN Legnaro as MB3 manufacturing site, the testing setup imitates a part of MB3 chamber front-end electronics. The 34 front-end boards are evenly split into two rows imitating two phi super layer front-end electronics of an MB3 chamber.

A simplified diagram of this testing setup is shown in Figure 4.1. Measurements involved two OBDT phi. One controlled the upper super layer, issued test pulses, and received hits. This OBDT phi was fully connected utilizing 15 front-end connectors and eight test pulse connectors. The second OBDT phi controlled only the lower super layer.

Communication with On-Board Drift Tube electronics was facilitated by an

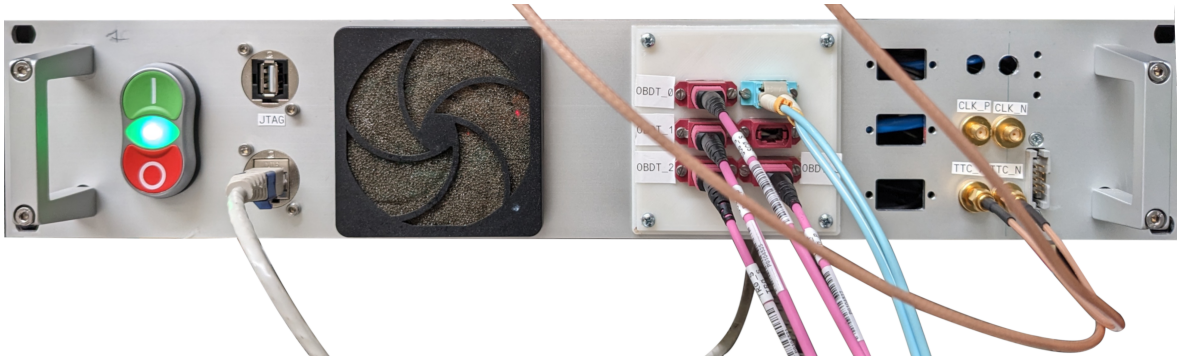

Figure 4.2: The figure displays the HTG box. The front panel of the box includes the connectors of the optical fiber cables necessary for communication with the On-Board Drift Tube electronics and backend.

FPGA board from the manufacturer HiTech Global (HTG) called HTG-940 [31]. Because HTG-940 houses a high-end field programmable gate array (either Virtex UltraScale or UltraScale+), it can support 10 Gbit/s communication over multiple channels [32, 33]. As mentioned in section 3.1, these requirements come from the low-power gigabit transciever protocol. HTG box houses the board and other electronics and services (Figure 4.2). The firmware running on the field programmable gate array incorporates protocols necessary for successful communication with the low-power gigabit transciever and Polarfire FPGA.

A server played an important role in the setup, executing the testing procedures and storing data. Similar to the communication with On-Board Drift Tube electronics, the data transfer between the server and testing electronics (HTG-940) also requires 10 Gbit/s speeds to accurately transfer the trigger data sent by On-Board Drift Tube electronics. The server runs the backend software for managing and logging the data from the HTG box.

The Wiring of the OBDT phi, as shown in Figure 4.3, features a fully connected OBDT phi in the center of the setup. Each OBDT phi front-end connector transfers 16 drift tube signals from one front-end board, so OBDT phi can monitor 240 drift tubes. The testing system used nine different front-end cable lengths shown in table 4.1. Coaxial cables of the same length transmitted the test pulses. Control of the front-end boards required a second OBDT phi highlighted in the left part of the picture. Each OBDT phi has only a single connector for the super layer and front-end board control. While additional OBDT phi and cables were present, they were not actively used in the testing process.

A special note needs to be taken for the slow control of the FEBs. Some specimens register the slow control signals as hits and generate fake hits. Because of this known fact, even the current operations of the Compact Muon Solenoid do not allow use of muon chamber slow control during data taking. This fact was rediscovered during the measurements at INFN Legnaro. The slow control of front-end boards runs at 100 kHz.

Table 4.1: A table showing the physical cable lengths of the OBDT phi front-end cables. Their dimensions are staggered in 15 cm increments. All lengths were used in OBDT phi tests.

OBDT phi front-end cable [cm]	25	40	55	70	85	100	115	130	145	160

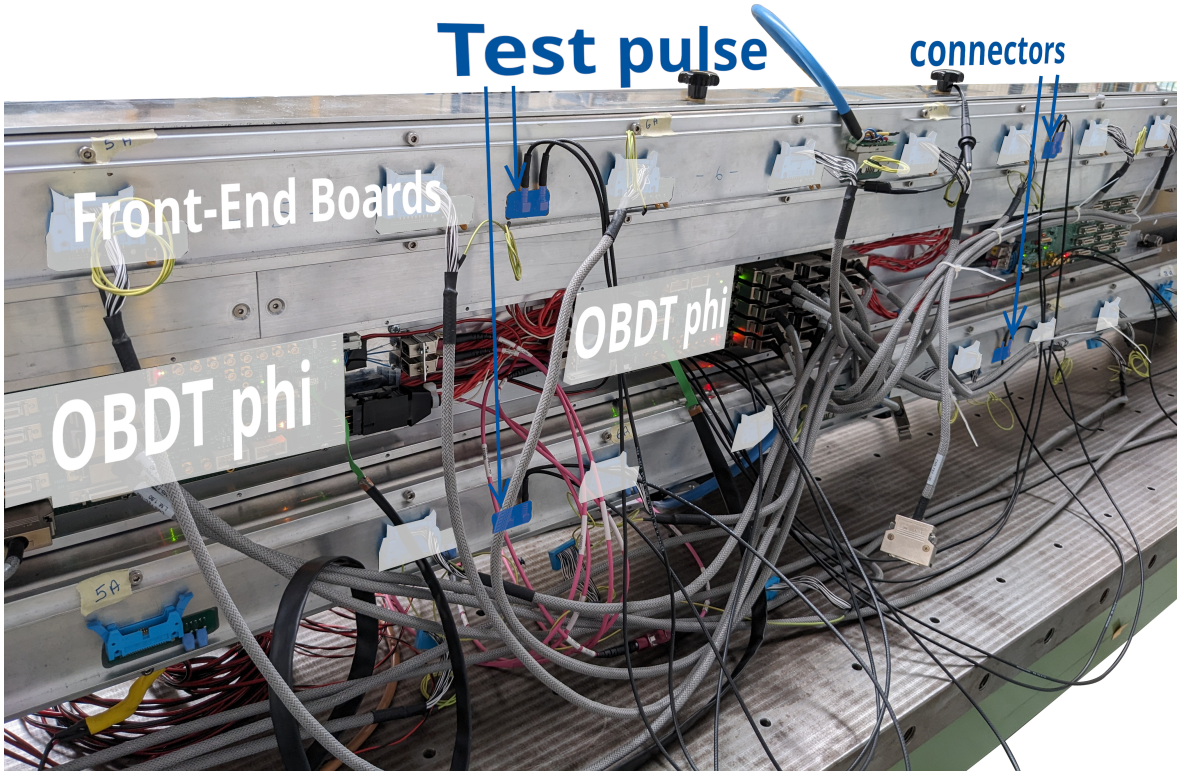

Figure 4.3: A picture that showcases the wiring of OBDT phi testing setup in Legnaro. Important parts of the picture are highlighted in white and blue. Both white OBDT phi controlled the highlighted front-end boards (FEBs). The orange color shows the super layer test pulse connectors.

4.3 Hardware used for testing of OBDT theta

Tests of OBDT theta were executed at CHARM [30], and only their analysis is the scope of this thesis. Apart from testing the theta version of the readout electronics, the irradiation tests included the Testpulse board, a front-end board, and a custom multiplexer. The multiplexer allows testing all test pulse connectors with just one front-end board. Compared to the testing campaign at INFN Legnaro, the backend incorporated the VCU 118 evaluation board with Virtex UltraScale+ FPGA and a laptop. The whole backend controlled On-Board Drift Tube electronics and recorded the data. Diagram 4.4 describes the experimental setup in greater detail.

Figure 4.5 displays the irradiated setup. Mounted on an aluminium stand, On-

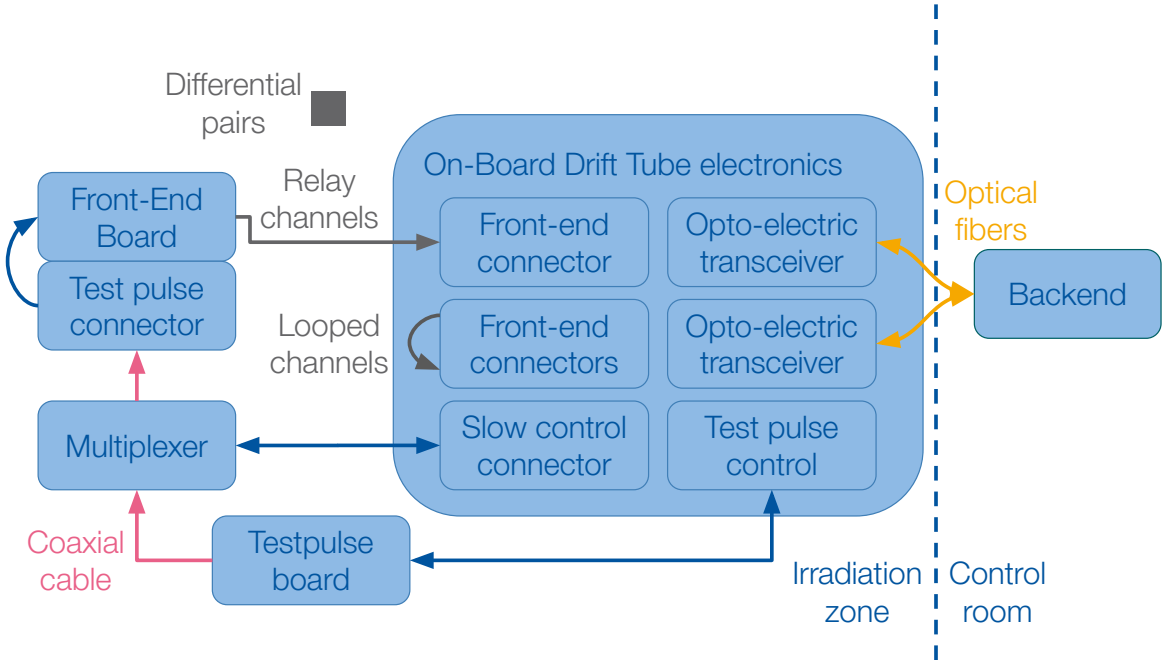

Figure 4.4: A diagram showing the experimental setup of the irradiation tests at CERN high energy accelerator mixed field facility. The OBDT theta controls the multiplexer and the Testpulse board, but it does not have access to the front-end board .

Board Drift Tube electronics, front-end board, the Testpulse board, and the multiplexer were air-cooled to guarantee constant temperatures. The electronics were exposed to a composition of neutrons, protons, and pions during the irradiation process [30]. For protection the backend electronics were shielded in the control room outside the irradiation zone.

The measurements at CERN high energy accelerator mixed field facility included two types of test pulse generation. Consequently, the analysis of the data distinguishes between two channel types. The single front-end board connects to the front-end connector 1 of OBDT theta (see Figure 4.6). Since the legacy front-end connectors concentrate 32 drift tube (DT) signals, only half of the connector was utilized. A total of 16 FPGA channels receive signals from one front-end board. They are further called front-end channels. The other six front-end connectors loop back to the read-out electronics. Because half of the connectors have to generate signals, only 96 signals are expected. FPGA channels receiving the 96 signals from the looped cables are further called looped channels.

Figure 4.6 clearly shows the wiring of the experimental setup. The design includes a series of looped connections between front-end connector, connector 2 linked to connector 3, connector 4 paired with connector 7, and connectors 5 and 6 joined together. Notably, connector 8 was not utilized. The optical lines from the Versatile Transciever Link plus opto-links run to the VCU 118, allowing slow control and faster trigger communication. The setup is completed with the VCU 118 connected to a laptop instrumental for recording data and controlling the system.

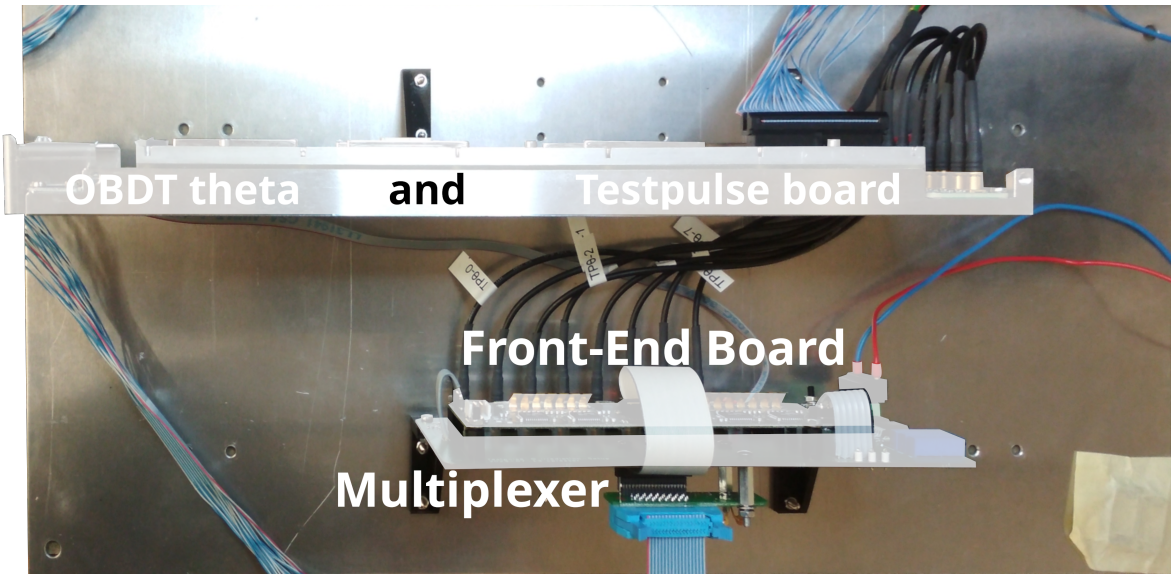

Figure 4.5: A picture of the electronics irradiated at CERN high energy accelerator mixed field facility. OBDT theta and the Testpulse board are mounted on an aluminium frame. Behind them stands a front-end board attached to the multiplexer (modified from [34]).

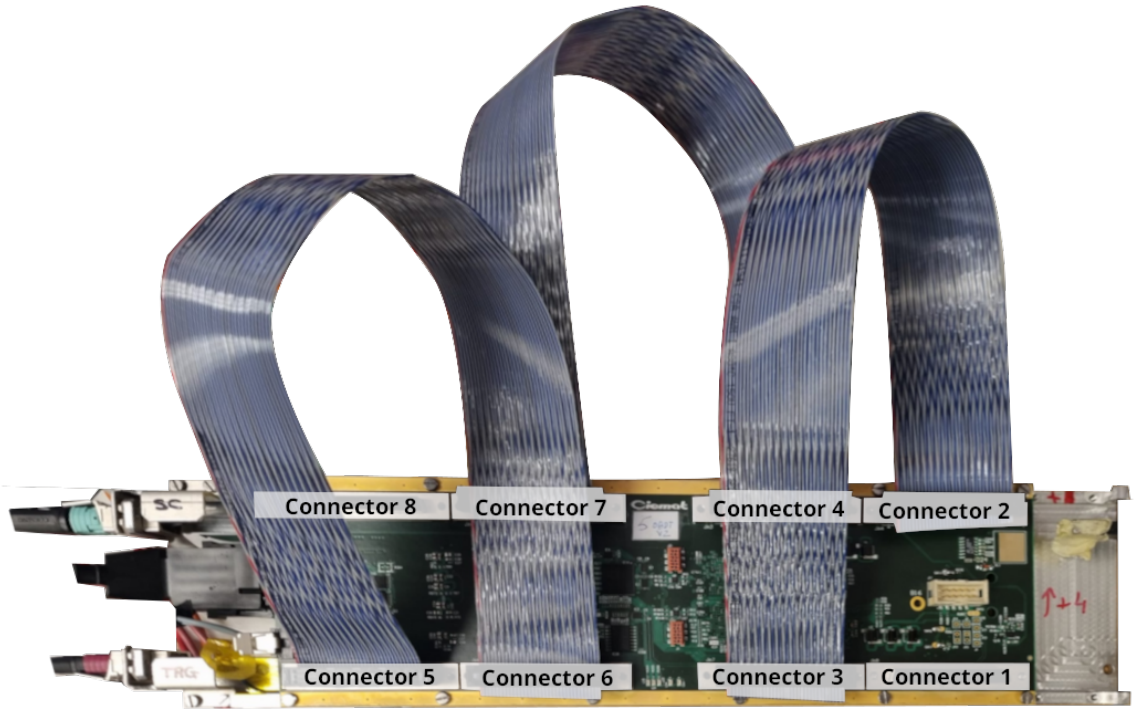

Figure 4.6: A picture that shows the OBDT theta looped channel wiring. The bottom right-most front-end connector received signals from the front-end board (modified from [34]).

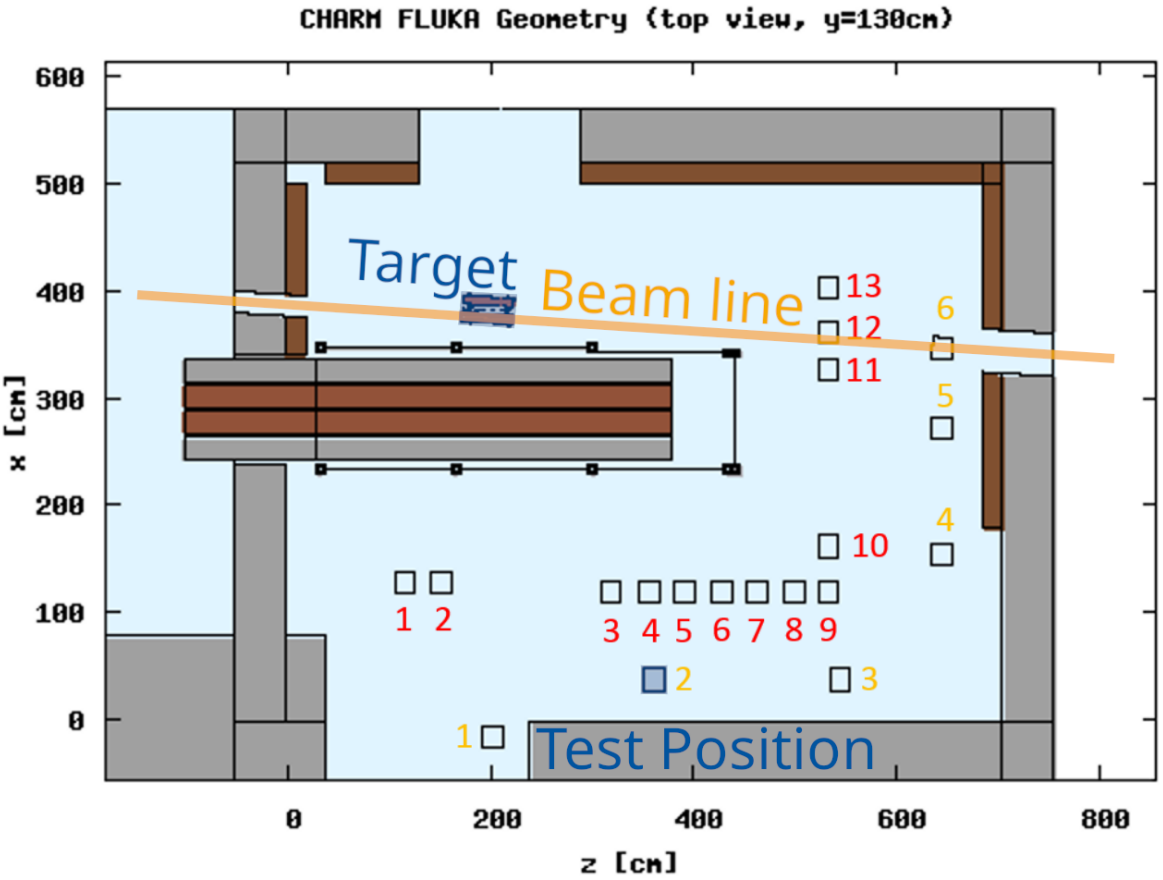

Figure 4.7: A technical sketch showing the irradiation room of CERN high energy accelerator mixed field facility. The orange line describes the beamline, and the blue highlights show the position of the target and the test position. In addition to concrete shielding drawn in gray, the room includes iron plates (brown). Through the center of the room cuts a removable shielding wall made of concrete and copper slabs. (modified from [30]).

Figure 4.7 illustrates the position of the tested electronics. Because the CMS muons system does not expect intense radiation, the electronics were strategically placed at stand number two, highlighted in yellow. This position is shielded from direct beam irradiation. As mentioned in section 3.5, On-Board Drift Tube electronics expects a dose of only 0.5 Gy during High-Luminosity LHC operations [22]. The removable wall in the irradiation room center shielded On-Board Drift Tube electronics, the Testpulse board, and the multiplexer to emulate the High-Luminosity LHC conditions.

Chapter 5

The results of On-Board Drift Tube electronics tests

The main scientific contributions of this thesis are highlighted in this chapter. Presented in two parts, jitter analysis begins the chapter. The first part focuses on OBDT phi jitter and the second on OBDT theta jitter. Spotlight then shifts to the long-term stability of the time-to-digital converter implemented in the OBDT theta. This section is particularly significant because the measurements were executed under irradiation, illustrating electronic operations during High-Luminosity LHC. Concluding the chapter is an exploration on the transmission limits of both OBDT versions. The section examines the transmission efficiency of On-Board Drift Tube electronics in parallel.

To present a more holistic picture of the On-Board Drift Tube electronics, the characterization tests looked not only at the rate capabilities of the electronics but also at jitter, time stamp drift, and detection efficiency. Achieving precise timing measurement requires jitter smaller than 0.78 ns (one bin resolution). Consequently, measuring the whole electronics jitter that limits the drift tube timing resolution is indispensable. Further, examination of the test pulse system should ensure excellent performance of a system responsible for timing calibration. Further, the time-to-digital converter performance expectations require minute-scale bin stability. The lowest benchmark specified for On-Board Drift Tube electronics demands time bin drift to take longer than one millisecond defined by the 16 orbits necessary to calibrate the entire drift tube system [35]. Finally, the OBDT phi was subjected to high hit rates to find its transmission limits, building upon the efficiency measurements of the slice test 3.4.

5.1 Jitter measurements

The Drift Tube system of the muon barrel system is an indispensable part of the CMS trigger. Therefore, the On-Board Drift Tube electronics has to provide precise timing information. Jitter significantly impacts the calibration of the timing system, so the test pulse system should produce a jitter below the resolution of the time-to-digital converter. Measuring the jitter then provides data that quantifies if the low jitter design effort succeeded. DT group did not set any benchmarks for the time stamp distribution. Nevertheless, calibrations of MB3 record the jitter standard deviation to be 1 ns, so this thesis adopts the current performance of the system as a benchmark [35].

5.1.1 OBDT phi jitter measurements

Data gathered for the jitter measurement originate from the testing procedure of OBDT phi described in section 4.1. An increased number of channels was activated after each test pulse. In order to increase the statistics on channels with a higher number all channels were pulsed multiple thousand times. Thanks to this addition the initial statistical difference between the channels becomes irrelevant. Expected sources of jitter include front-end boards, thermal noise, and the test pulse system.
According to past calibration measurements, the recorded time stamps should produce histograms about 4 time bins wide (1 ns standard deviation). Created by the test pulse system, the time stamps are expected to fall within 25 ns bunch crossing similar to the past measurements in [35].
Figures 5.1 and 5.2 represent jitter measurements of OBDT phi. The histograms display two types of timestamp distributions observed across the 240 channels. Each time stamp distribution has a mean described by the term channel average. Time stamps beyond one bunch crossing (25 ns-cutoff) appear because they ranged over two bunch crossings.
The histogram 5.1 shows that four bins received more than 1000 hits. An asymmetric tail pointing towards higher times comprises five hits. Compared to the 8700 hits sent to channel 8, the five hits in the distribution tail constitute a statistically insignificant amount. Its standard deviation falls slightly below 1 ns.
Comparing the type of distribution in Figure 5.1 to past measurements shows agreement with MB3 jitter. Only 4% of channels display similar distributions. Front-end boards, the test pulse generation, and thermal noise are responsible for the observed jitter.
Figure 5.2 shows the second type of timestamp distribution. The histogram has a similar distribution around the data median. Three bins reach above the 2100-hit mark, and the fourth bin tallies close to 1000 hits. Finally, the standard deviation of this type of distribution reaches slightly above 1 ns.
A similar jitter width appears in the both types of time stamp distribution demonstrated by Figures 5.1 and 5.2. Because of the unconventional time stamp distribution shape, the majority of jitter most likely originates from electronics and not from thermal fluctuations. Reaching a measure slightly higher

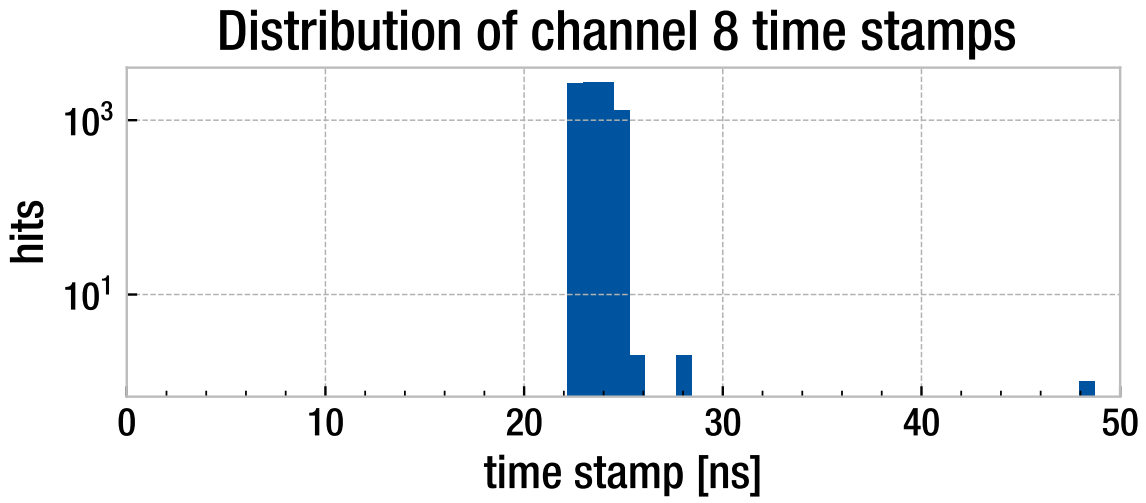

Figure 5.1: A cumulative histogram that shows all time stamps recorded from channel 8. The x-axis shows the nanosecond value of the time stamp spread over two bunch crossings. The y-axis has a logarithmic scale and describes the number of hits received in a specified 0.78 ns time bin. The data were recorded by OBDT phi.

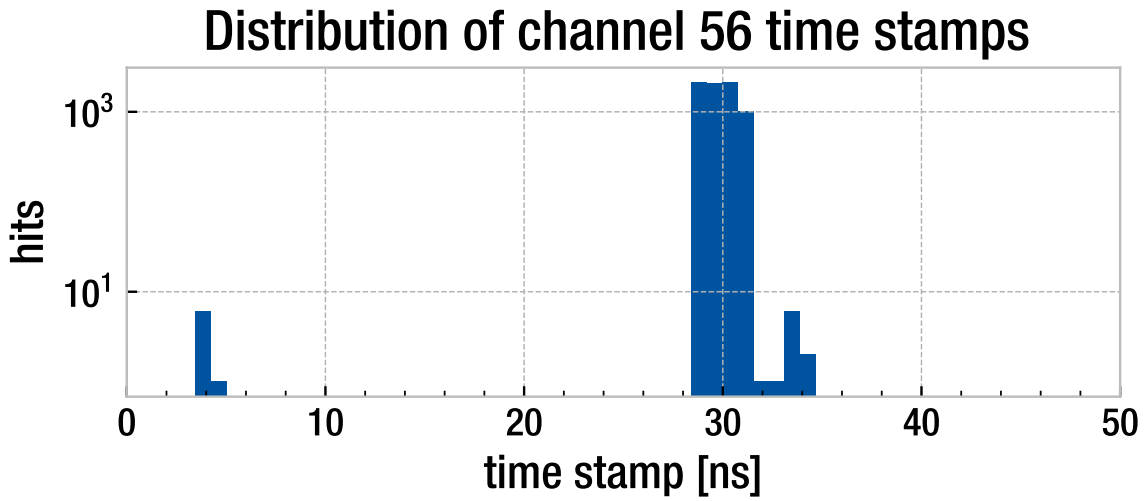

Figure 5.2: A cumulative histogram that shows all time stamps recorded from channel 56 by OBDT phi. The x-axis shows the time stamp values across two bunch crossings. The y-axis has a logarithmic scale and describes the number of hits received in a specified 0.78 ns time bin.

than the past measurements, almost 66% of the channels still fall within expected jitter values.

An outlying noisy channel is shown in Figure 5.3. Reaching the width of more than 6 ns, the peak of the distribution spreads around the 44 ns-mark. The main peak reaches about 6700 hits. About 28% of other channels experience jitter with similar standard deviation as the main peak. In addition to the main peak, the distribution also has a second peak around the 17 ns-mark. Totaling

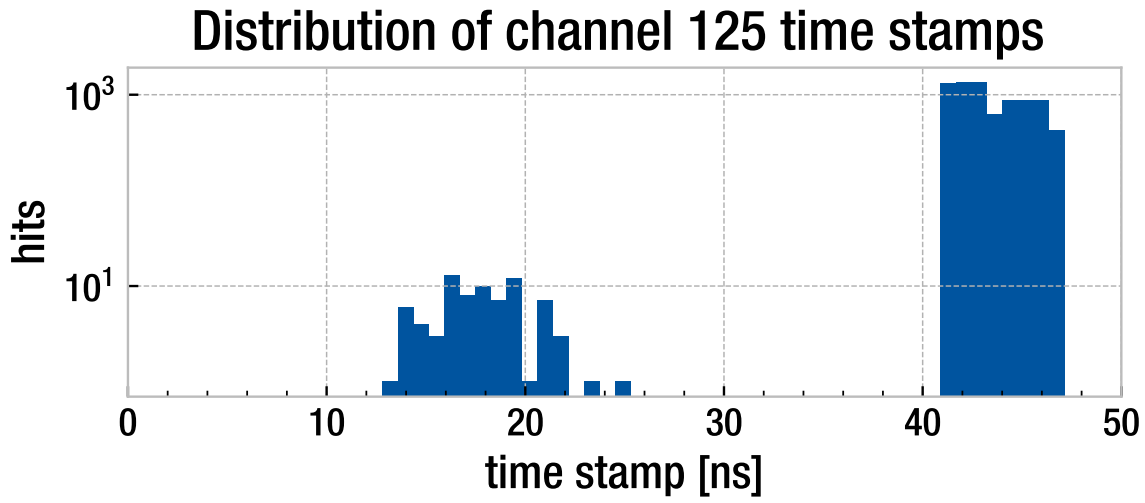

Figure 5.3: A cumulative histogram that shows all time stamps recorded from channel 125. The x-axis describes the time stamp value. The y-axis has a logarithmic scale and describes the number of hits received in a specified 0.78 ns time bin. Two distinct distributions in the histogram include more than 70 (left) and close to 6700 (right) hits. The data were recorded by OBDT phi.

more than 70 hits, the distribution reaches a width of almost 8 ns.

The two distributions observed in Figure 5.3 exemplify random and deterministic jitter. The left distribution closely resembles a Gaussian curve characteristic for jitter caused by thermal fluctuations. The left distribution is an example of a deterministic jitter caused by the electronics. Channel 125 exemplifies why front-end boards includes a masking system capable of disconnecting individual channels from the read-out. The masking mechanism ensures that the data flow does not saturate with non-physical data.

Figure 5.4 shows the complete jitter measurement summary of the OBDT phi. All distributions were shifted to the channel average. Moving all distribution towards a common mean illustrates a distinct pattern in the recorded jitter. 66% of distributions have their standard deviation larger than 1 ns (See appendix A for the plot of the channel standard deviations.). Many also include hits recorded outside of this width with less significant statistics.

The majority of channels exhibit jitter with its standard deviation close to 1 ns. Thus, the channels do reach the jitter expected from [35]. Some channels, 28% exactly, reach higher jitter. High jitter creates costly ambiguity detrimental to the drift tube special resolution. The large test pulse jitter does not allow accurate time calibration. Drift tube response time spans multiple bunch crossings and combined with pileup, a large calibration uncertainty can result in false muon track reconstruction.

The high-radiation environment cannot produce the jitter because the measurements were not executed in a high-radiation zone. Also, the front-end boards used for the Minicrate test stand in Legnaro were not irradiated and were not used at the Large Hadron Collider. Therefore, the measured jitter does not originate from radiation-induced electronics degradation.

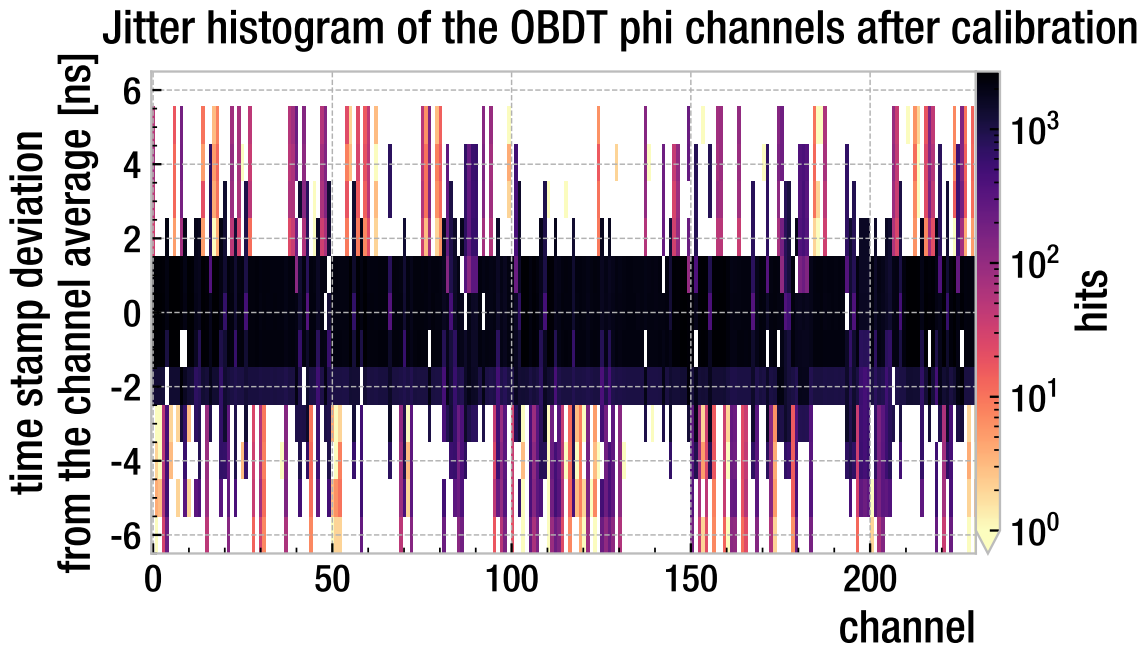

Figure 5.4: A two-dimensional histogram summarizing all the noise measurements of OBDT phi. The time stamp distributions were shifted by their averages. The x-axis describes the channel number, the y-axis the distance from the mean of the distribution and the logarithmic color scale describes the number of hits in a bin.

The intrinsic drift tube time fluctuation does not produce the observed jitter either. Although the drift tube jitter width of 3.1 ns, roughly four bins, fits with the observed data, the front-end boards did not receive any signals from drift tubes (DTs) [17]. The testing setup included only the front-end boards.

Similarly, the measured jitter cannot be internal because TDC performance was already labeled satisfactory in [23]. Established in section 3.5 Figure 3.8, the differential non-linearity of the time-to-digital converter in the FPGA reach below 10%. Translating to 10% of 0.78 ns, the data contradict the notion that OBDT front-end lines could produce 4-bin or 3.12 ns wide jitter. Lastly, channel crosstalk has even smaller effect on time digitization (Figure 3.9 section 3.5) and does not significantly contribute to jitter observed in 5.4.

The jitter most likely originates from the front-end boards (FEBs). The front-end board design has not changed since the muon chamber manufacturing. Combined with electronics aging, the front-end boards (FEBs) can easily suffer a slight jitter increase. The global standard deviation of OBDT phi jitter accounts to 1.37 ± 0.33 ns.

Figures 5.5 and 5.6 examine the jitter further. Without shifting the distributions, a more complex and information-rich picture arises in the two-dimensional histogram 5.5. Channels build groups. Broad rising and falling trends appear in the histogram and a small number of hits rests downshifted by one bunch crossing. However, the majority of hits were recorded in the "second" bunch crossing, i.e. after the 25 ns-mark. The channel time stamp average, or chan-

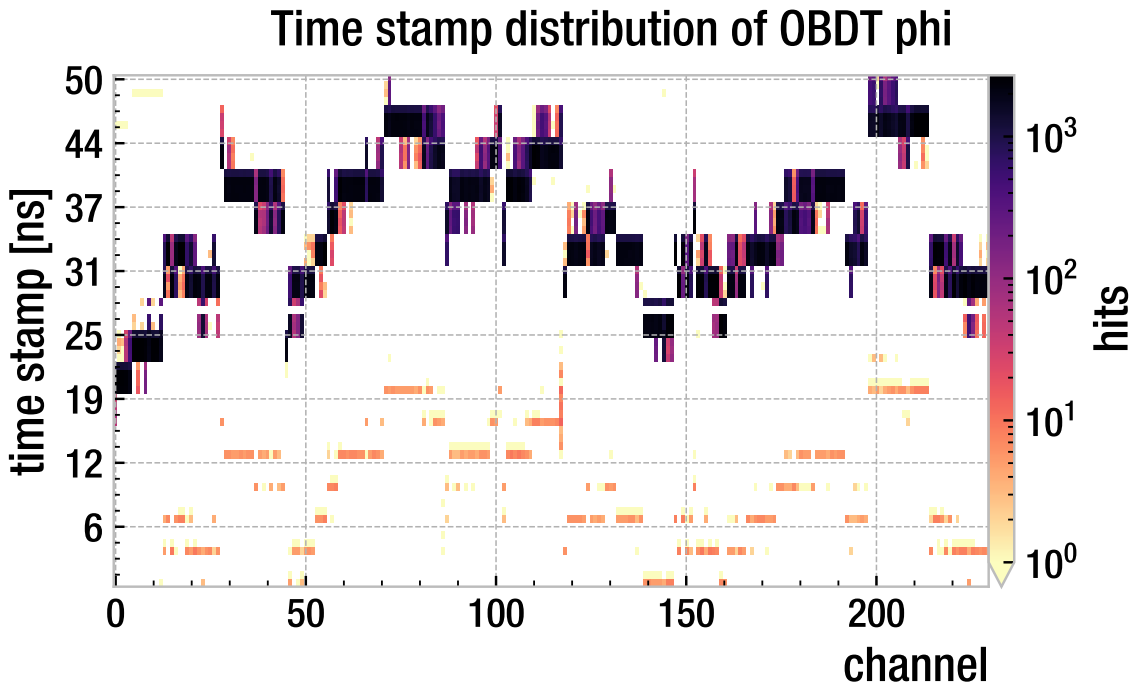

Figure 5.5: A two-dimensional histogram that describes the time stamp distribution of the OBDT phi tests. The x-axis describes the channel number, the y-axis the timestamp value in nanoseconds, and the logarithmic color scale describes the number of hits in the bin.

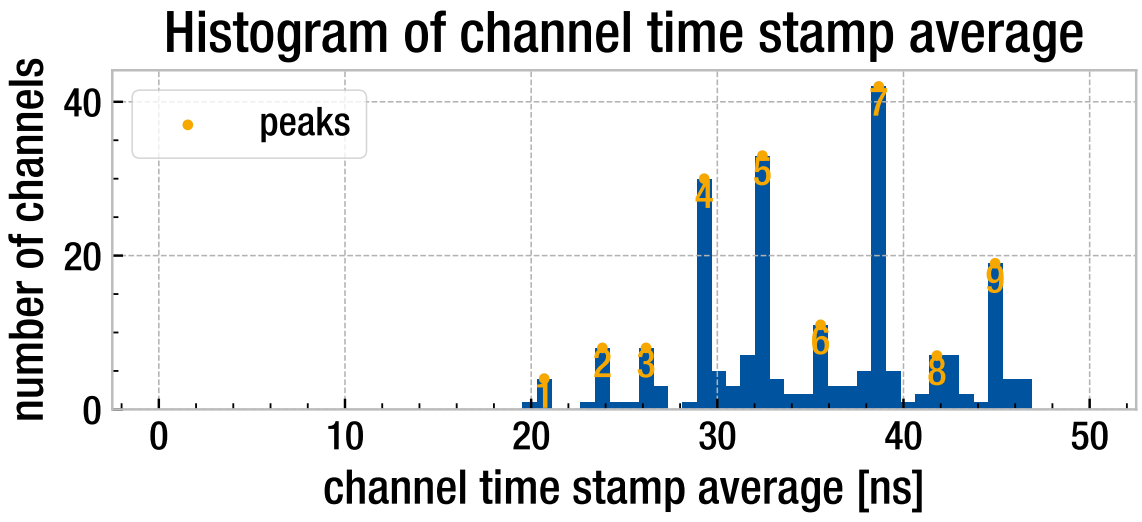

Figure 5.6: A histogram showing the stacking of all time stamp distribution means. The x-axis describes timestamps in nanoseconds. The y-axis shows the number of channel means in a given time bin. The differences between the peak x-positions should correspond to front-end cable lengths.

nel average, distribution spreads across almost 27 ns.
The grouping of the time bins suggests that the OBDT phi FPGA receives the signals in a length-matched design. Because signals went through nine different cable lengths, the time stamps can appear in nine subgroups. Consequently, the dominant effect responsible for the widespread of the time stamp distributions are front-end cable length differences.
To examine the signal path differences further, the means of the time stamp distributions can be histogrammed. Figure 5.6 shows this histogram. The histogram includes multiple peaks. Starting at 20 ns, channel average distribution produces nine peaks and ends at 47 ns.
Building time differences between the peak 1 and the other peaks gives an examination method for the OBDT phi and its jitter. According to the experimental setup described in section 4.2 the differences between the peaks of the distribution in Figure 5.6 should come from the cable length differences. The relative times give information about the signal path differences within the system.
The time differences Δt in table 5.1 range from 3.1 ns to 24.2 ns. Nine total peaks create nine groups matching the number of cable lengths in the setup. Test pulse cables had the same length so the differences must originate from the front-end cable length variation. When time differences are translated to signal path length differences Δl, they do not match the physical cable length differences. Using the speed of light at 0.3 m/ns and assuming the signal propagation reduction in copper to be very conservative 40%, the length differences reach more than 4 meters. Compared to the actual cable length differences, the supposed lengths reach values from more than three- to almost four-times larger.

Table 5.1: Table comparing the physical and measured path length differences based on the relative time differences. The computation of length differences assumes the speed of light as 0.3 m/ns and a conservative 40% reduction of the speed in copper.

Δt [ns]	$\Delta l_{measured}$ [m]	$\Delta l_{physical}$ [m]
3.1	0.6	0.15
5.5	1.0	0.30
8.6	1.5	0.45
11.7	2.1	0.60
14.8	2.7	0.75
18.0	3.2	0.90
21.1	3.8	1.05
24.2	4.4	1.20

Multiple reasons might explain the observed three- to almost four-times larger path length differences. First the OBDT phi test pulse system might be at play. If OBDT phi does not generate the pulses simultaneously, the nanosecond

delays add to the path differences. Second, the incorrectly initialized input delays of FPGA inputs or firmware bugs might also produce several nanosecond differences in arrival times. Front-end cable length differences also add to the path length differences contributing a few nanoseconds. The mentioned phenomena create the distribution observed in the histogram 5.5. The results suggest tweaks to OBDT phi firmware or the use of the OBDT theta version. Further, the jitter of the OBDT phi system would benefit from decrease.

5.1.2 OBDT theta jitter measurements

Gathering data for the OBDT theta jitter measurement was described in section 4.1 in greater detail. In short, all monitored channels were continuously pulsed during the entire four-day measurement. A single channel accumulated around 10^7 timestamps and experienced irradiation during the entire data taking. The recorded time stamps then serve as data for analyzing the electronics jitter. Expected sources contributing to jitter include the Testpulse board, multiplexer, and front-end board. Similarly to the OBDT phi measurements this analysis carries the 1 ns standard deviation jitter as a point of comparison.
Focusing on the jitter measurements of OBDT theta, the time stamp distribution of these electronics spans over 25 ns. Compared ot OBDT phi jitter measurements in section 5.1.1, the spread of the time stamps did not reach two bunch crossings. The first type of timestamp distribution illustrated by Figure 5.7 shows a distribution with almost 0.3 ns standard deviation. The channel 35 stimulated with test pulses passing through line one of the multiplexer has a distribution centered around 14 ns. The histogram in Figure 5.7 represents nine of the time stamp distributions that originate from front-end channels.
The distribution type shown in the histogram is narrower than most OBDT phi distributions. Therefore, the jitter performance of the tested system compares exceeds the past MB3 measurements presented in [35]. Compared to the majority of OBDT phi timestamp distributions, the recorded distribution is one bin thinner.
Less than a half of front-end channels, i.e. less than 40%, experience larger jitter. Demonstrated by the histogram in Figure 5.8, their distribution standard deviation reaches around 1.5 ns. The distribution shows double peaks centered around 19 ns. Positioned close to 18 ns, the first peak reaches statistics of more than 10^5 time tamps. The second of the double peaks represents more than 10^7 hits.
The second distribution type of the front-end channels closely resembles OBDT phi jitter. Its 0.4 ns standard deviation creates almost expected timing ambiguity. Compared to the 1 ns standard deviation, the six front-end channels show better jitter still.
Figure 5.9 demonstrates distribution types with two distinct peaks. In this exact example the higher peak one spreads around 16 ns and the second around 19 ns. Both peaks have similar widths, below 1 ns, but the second peak reaches a statistic two orders of magnitude smaller than the first higher peak. This type of distribution appears for all channels receiving signals through the multiplexer relay 6.

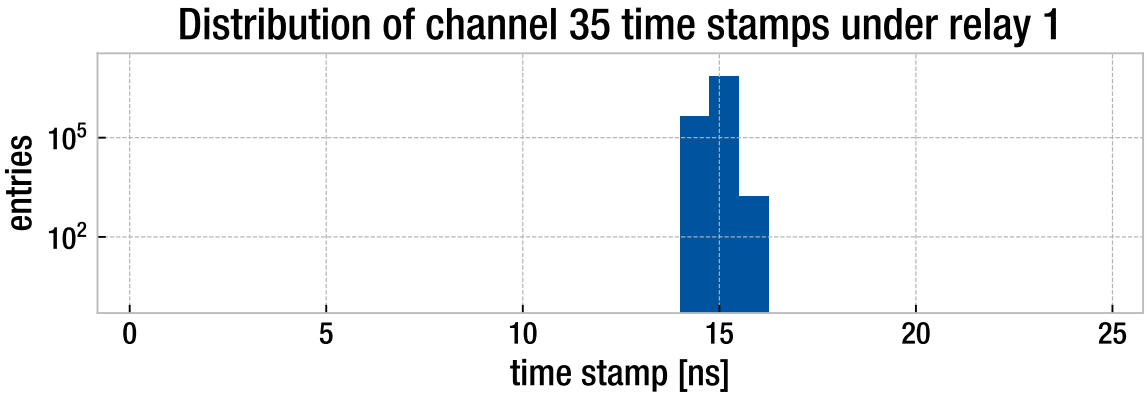

Figure 5.7: A cumulative histogram that shows all time stamps recorded from channel 35 by OBDT theta. The x-axis describes the time stamp values. The y-axis has a logarithmic scale and describes the number of hits received in a specified 0.78 ns time bin.

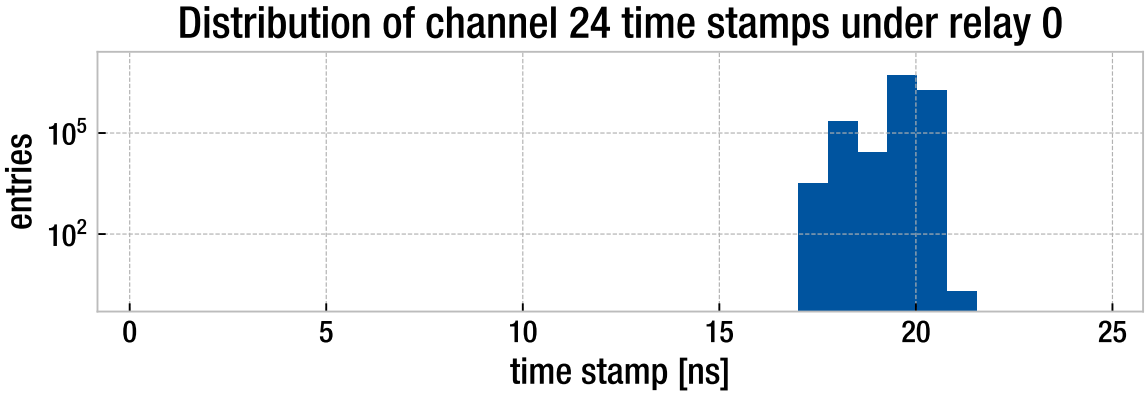

Figure 5.8: A cumulative histogram that shows all time stamps recorded from channel 24 under relay 0. The data were recorded by OBDT theta. The x-axis shows the time stamp bins. The y-axis has a logarithmic scale and describes the number of hits received in a time bin.

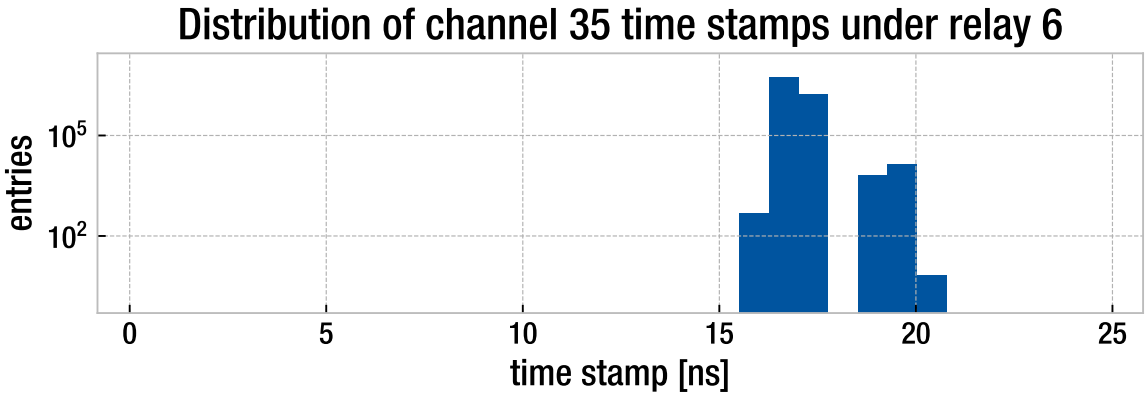

Figure 5.9: A histogram that shows all time stamps recorded from channel 35 under relay 1. The x-axis describes the time stamp values. The y-axis has a logarithmic scale and shows the number of hits received in a time bin. The data were recorded on OBDT theta.

Since the data come from the channel 35, the same channel as in Figure 5.7, the observed effect can be attributed to the multiplexer lines. The only difference between Figure 5.7 and 5.9 are the used test pulse lines. Combined with the observation of the behavior across all front-end channels connected through the multiplexer relays 6, test pulse line has to be responsible for the observed distribution type in Figure 5.9.

Possible explanations for the observed double peak distribution include time bin jump and reflections. Similar to previous explanations the time bin jump most likely originates from the radiation environment. The reflections could arise in the multiplexer from incorrect impedance matching of the test pulse lines.

Jitter measured in the front-end channels also does not stay completely within one 0.78 ns time interval. Considering the statistics, the OBDT theta experience slightly less jitter than OBDT phi. The measurements not only compare the On-Board Drift Tube electronics versions but also their test pulse systems: the Testpulse board for OBDT theta and an integrated system for On-Board Drift Tube electronics (OBDT) phi. The largest distribution widths for a given line reach about 3 ns (Figure 5.8).

The jitter can originate from the used electronics or thermal noise. Determining the origin of the jitter is difficult for three-bin-wide distributions. For channels 24 to 29 the shape of the distribution suggests that the jitter originates from the electronics. Because the Testpulse board and the multiplexer were wired in series, the data does not allow determining which piece of these electronics causes this behavior.

The wider distribution in Figure 5.9 does not originate from the front-end board or the Testpulse board. Because both Figure 5.7 and 5.9 show the same channel stimulated by a different signal coming from the multiplexer.

The final two types of jitter histograms come from the channels looped from one front-end connector of OBDT theta to another (section 4.3). Figure 5.10 depicts the ideal case of time distribution of only one time bin at 16 ns. The logarithmic y-axis only reaches the 10^7-mark. Focusing on the statistics of the measurement, channel 216 recorded almost $5 \cdot 10^7$ hits.

Figure 5.10 illustrates single bin jitter. Confirming the DNL measurements in section 3.5 Figure 3.8, the histogram demonstrates the low internal jitter of OBDT theta. The jitter introduced by the two front-end connectors in combination with internal jitter capped by the maximum 10% DNL measurement stays under of 0.78 ns.

The second type of behavior of looped channels surfaces in Figure 5.11. Time stamps of channel 222 spread over two bins giving the distribution a width of 1.5 ns. Both bins reach more than 10^7 hits with a difference of $8 \cdot 10^6$, and the distribution mean lies at the 19.5 ns mark.

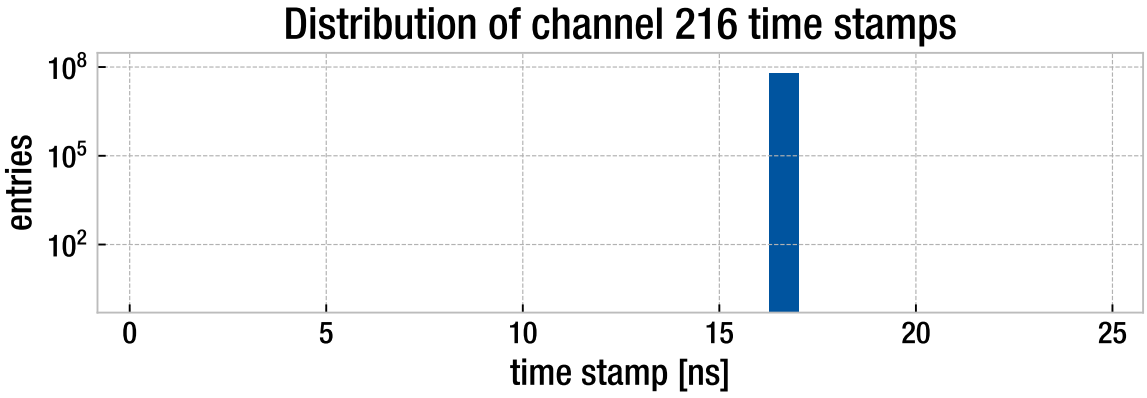

Figure 5.10: A cumulative histogram that shows all time stamps recorded from looped channel 216. The x-axis describes the nanosecond value of the recorded time stamps. The y-axis has a logarithmic scale and describes the number of hits received in a specified 0.78 ns time bin. The data were recorded on OBDT theta.

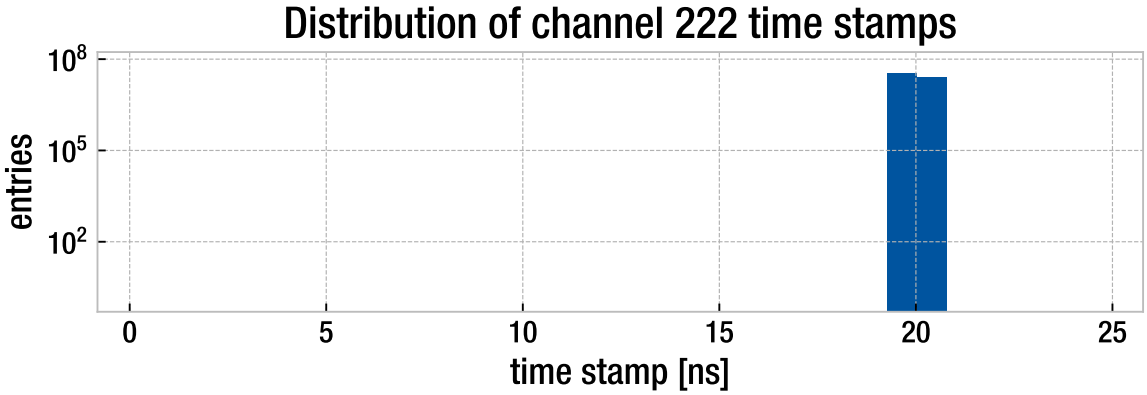

Figure 5.11: A cumulative histogram that shows all time stamps recorded from looped channel 222. The data were recorded on OBDT theta. Time stamp values are depicted on the x-axis. The y-axis has a logarithmic scale and describes the number of hits received in a specified 0.78 ns time bin.

Considering the achievable low jitter measured in channels such as 216, the distribution in histogram 5.11 might not come from an increased jitter. An alternative explanation for the shown distribution might come from a time drift of the generated FPGA clock. If signals arrive closer to the time bin edge, a slight change in frequency causes the pulse to fall into a different time bin.

As in the case of the jitter analysis of OBDT phi, all distributions appear in the jitter histogram 5.12. Most looped channel distributions span only one time bin. Thirteen channels exhibit mostly one time bin distribution, having only few hits around the main bins. Finally, 27 channels show a distinct two-bin time stamp distribution.

All distributions at once can be seen in the two-dimensional histogram 5.13. No observable trends appear in the histogram. 46 of the jitter distributions

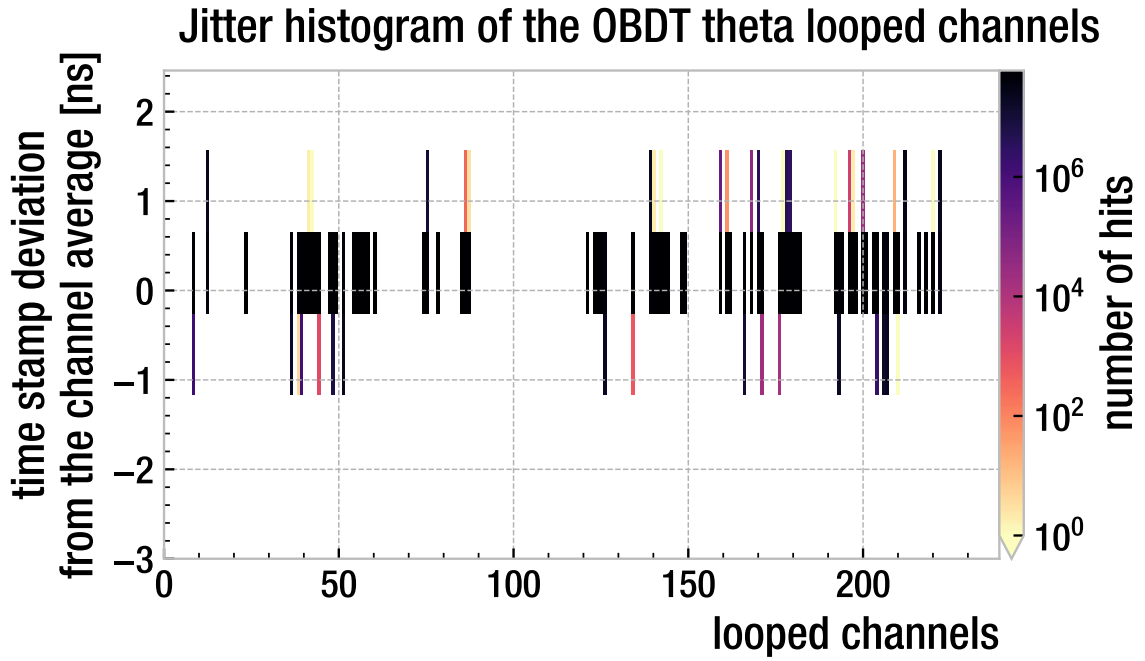

Figure 5.12: A two-dimensional histogram that shows the jitter widths of the OBDT theta looped channels. All distributions center around their maximum bin. Looped channel numbers are depicted by the x-axis and the deviation of the time stamp from the channel maximum by the y-axis. The color logarithmically describes the number of hits in a bin.

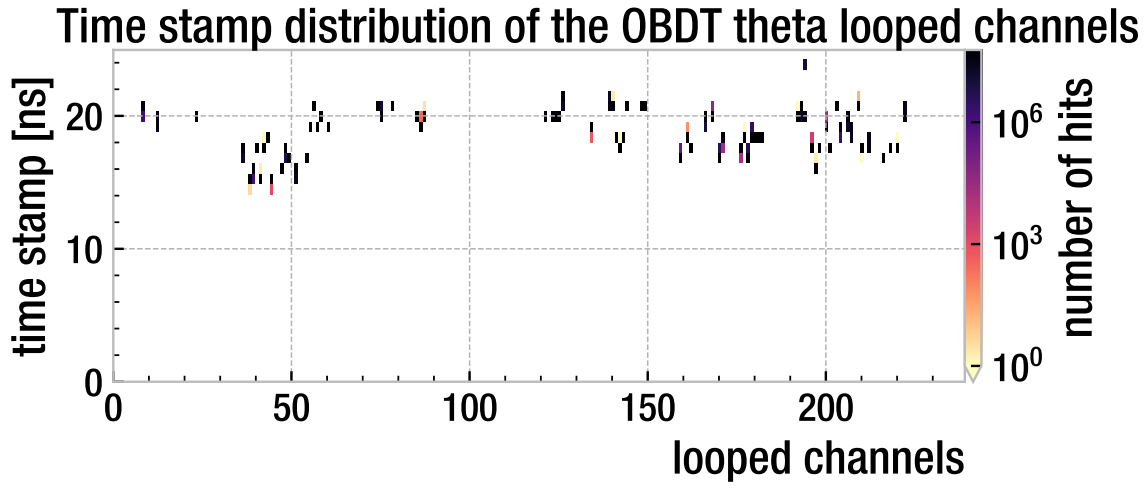

Figure 5.13: A two-dimensional histogram that shows the distribution of the OBDT theta looped channel. The x-axis describes the looped channel numbers, the y-axis the time stamp value, and the color describes the number of hits in the bin.

spread over a single time bin, and 27 include a significant amount of hits in the second time bin. The spread of the distributions approaches 9 ns.

The looped channels show excellent jitter behavior. The majority of looped channels received one-bin-wide time stamp distribution over four days. They show excellent timing stability in a radiation environment. The other looped channels exhibit a two-bin-wide distribution. Compared to the jitter measured on the OBDT phi system, the width shows promising results nonetheless. Bin drift could explain the the two-bin wide distributions. Nevertheless, the wiring that produces the excellent jitter does not include front-end boards, making the measurements less relevant for High-Luminosity LHC operations.

The combined jitter information of front-end channels appears in the jitter histogram 5.14. Only channel five reaches two time bin jitter. The other channels experience wider distributions: 56% have three-bin-wide; almost 19% are four-bin-wide, and more than 18% have five-bin-wide timestamp distributions.

Examining the jitter histogram of the front-end channels, the front-end channels exhibit more jitter than the looped channels. Because the channels receive their signals from a more complex system, the variety of the observed distributions is also larger than in the case of looped channels. The three bin wide distributions show an expected jitter. Bin jumps from single event upsets might cause the wider time stamp distributions.

Centering the distributions around their maximum bin does not change the general look of the distribution. This fact shows time stamp behavior consistent with the wiring of the experimental setup. All 16 signals travel through a front-end cable of the same length. Next, the test pulse activates all channels at the same time. Finally, the time stamp distribution demonstrate that the input delays of the field programmable gate array create no measurable difference.

Combining jitter histograms of front-end and looped channels the Figure 5.15 demonstrates the difference between the channels types. The front-end channels have bins with ten-times less hits because the multiplexer relay 3 closed only for a set portion of the measurement. Their distributions exhibit standard deviations greater than those of the looped channels, but both reach values below 0.5 ns (see appendix A for plot of all standard deviations). The OBDT theta setup thus shows outstanding timing stability.

Jitter measurements of OBDT theta show excellent results. Although looped channels exhibit excellent time stamp distribution widths, they do not represent a realistic scenario for the test pulse system. All front-end channels, on the other hand, display an first-class jitter. The standard deviation of all time stamp distributions reaches below 0.5 ns. Compared to the MB3 measurement from [35] that describe the time stamp distributions to have standard distribution around 1 ns, the averaged front-end channel time stamps standard deviation of 0.32 ± 0.13 ns falls well below the comparison point of 1 ns.

Moreover, the OBDT theta jitter is also smaller than the OBDT phi jitter. The comparison derived from the jitter measurements shows that OBDT theta uses a test pulse system with greater timing stability. Similarly to the OBDT phi mea-

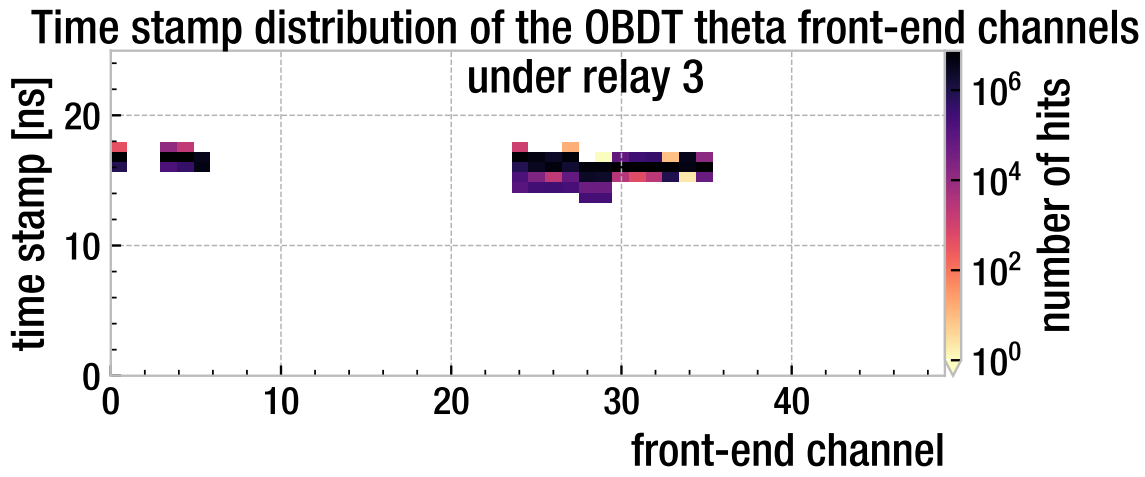

Figure 5.14: A two-dimensional histogram that shows the time stamp distribution of front-end channels of OBDT theta. The data from the entire four-day measurement campaign are plotted such that the x-axis describes the relay channel number; the y-axis shows the time stamp value; and the color describes the number of hits in a given bin.

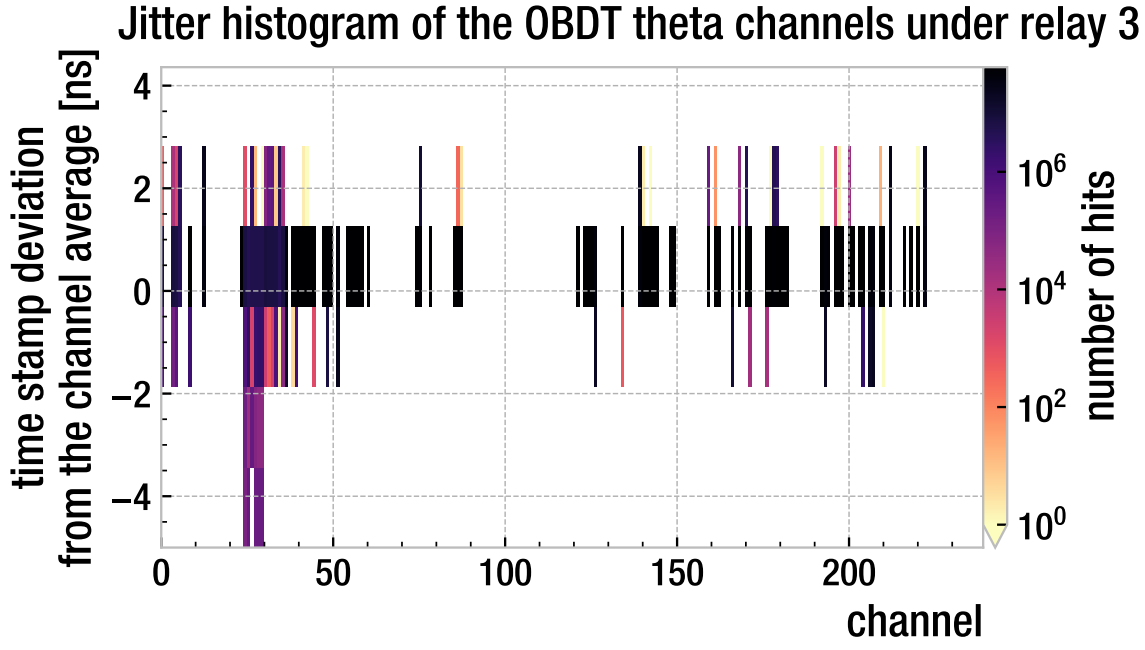

Figure 5.15: A two-dimensional histogram that combines jitter of looped and front-end channels of OBDT theta. The channels are described by the x-axis and the time stamp value by the y-axis. The logarithmic color-scale describes the number of hits in a bin.

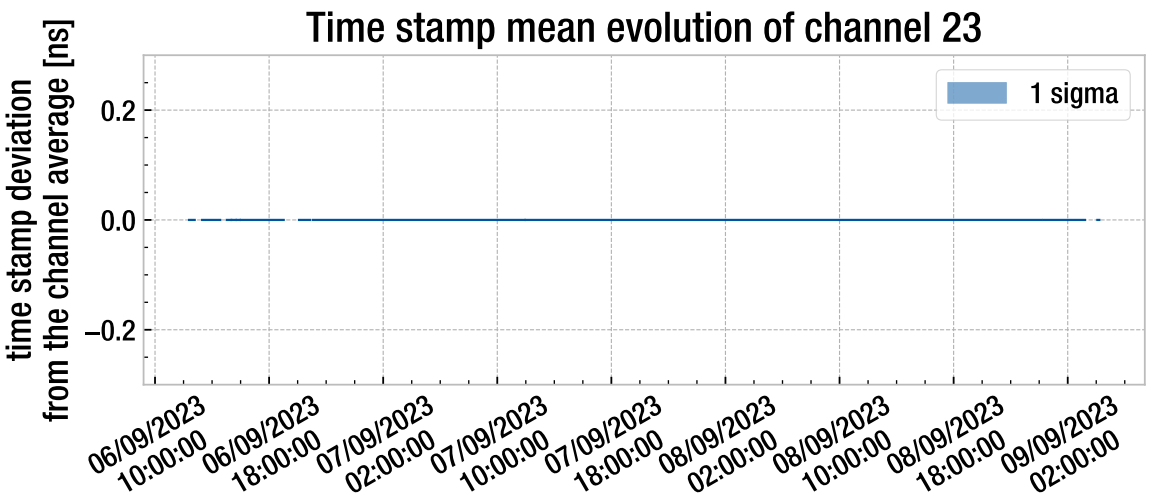

Figure 5.16: A plot depicting the ten-second average of time stamps recorded for channel 23 by OBDT theta. The y-axis of the plot shows the deviation of the time stamps from the channel average in nanoseconds, and the x-axis depicts the date and time of the measurement.

surements the jitter sources in OBDT theta measurements include front-end boards, the test pulse system, thermal noise, and additionally the multiplexer. Spread of the time stamp distributions also falls within one punch crossing as expected from [35].

5.2 Stability of the time-to-digital converter

Measurement campaign at CERN high energy accelerator mixed field facility required continuous monitoring, so its data allowed examining the performance of the time-to-digital converter implemented on the OBDT theta FPGA. Channels are considered to be stable if the mean of their time stamp distribution does not drift more than 1.56 ns over 1.4 ms [35]. A more practical requirement would push the 1.4 ms necessary to calibrate the whole drift tube system during 16 abort gap cycles to a few minutes.
Since jitter gives only a snapshot of time stamps for a given time interval, it cannot distinguish whether the time distribution comes from random noise or a systematic drift. To disentangle these effects, this thesis examines stability of the time-to-digital converter implemented in the OBDT firmware by studying the evolution of channel timestamp distribution means over time.
Figure 5.16 shows the time stamp distribution mean, or time stamp mean, evolution of channel 23. In fact, channel 23 represents the majority of looped channel behavior. The timestamp mean stays within the same bin over four days exemplifying the ideal time stamp behavior with no timestamp drift.
The plot thus supports the jitter measurements (Figure 5.10). Almost 72% of the looped channels remain exceptionally stable in the four-day measuring period. The standard deviation plotted in Figure 5.10 remains almost zero because all signals were recorded in one time bin.

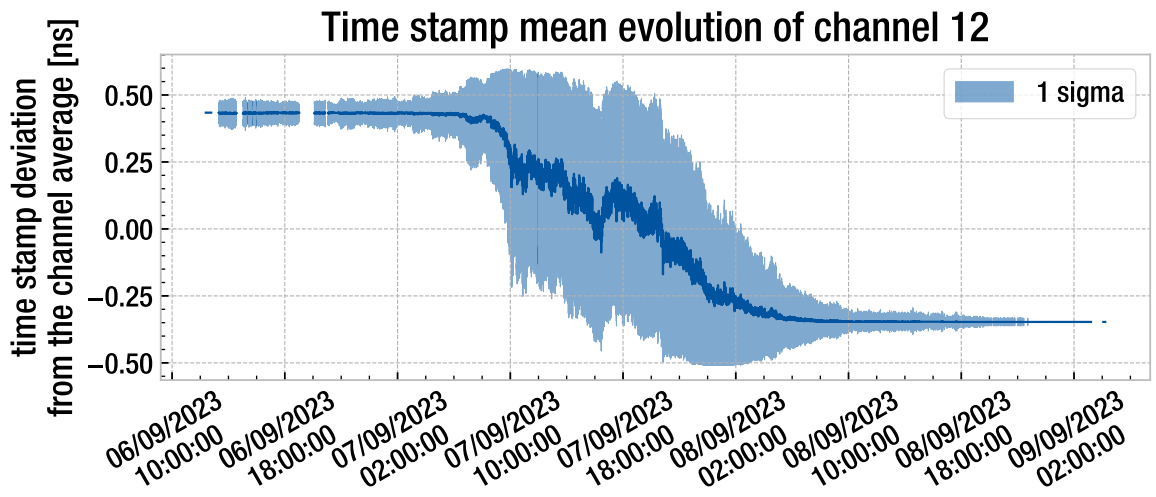

Figure 5.17: A plot demonstrating the time stamp drift measured by OBDT theta. The ten-second timestamp mean was recorded for channel 12. Measurement time is described on the x-axis, and the deviation of the time stamp mean from the channel average is on the y-axis.

Apart from the channels with no timestamp drift, the measurements also found 19 channels that do drift. Shown in the example of channel 12 (Figure 5.17), the plot describes a one time bin drift of the time stamp mean. Magnified by the increase in standard deviation, the drift happens over the course of one day starting after 7:00 on the 7th and ending before 7:00 on the 8th of September. The present time bin drift explains the two-bin jitter width of several looped channels. If the signals from front-end boards arrive close to the bin edge, the time-to-digital converter can record them in one or the other bin with a given probability. Because the reference clocks in the field programmable gate array experience drift, their change of frequency can lead to measuring the signal arrival time in a different bin.

Channel 194 is one of two outliers and exhibits a time bin jump of almost 4 ns for almost eight and a half hours (Figure 5.18). The time bin jump shown in Figure 5.18 creates two domains with constant timestamp value and same close to zero standard deviation. The second channel that experiences time bin jump is the channel 171. Reaching magnitude of almost 2 ns the time bin jump does not last for a prolonged time span. The rest of data fall withing one time bin.

Only two channels experienced this behavior. Making barely 3% of all monitored looped channels, they both highlight the need for online monitoring. Combined with the radiation environment that OBDT theta was exposed to, this behavior can be attributed to time bit jump caused by single event upsets. The time bin jumps also justify frequent recalibration of the timing system in order to maximize the data taking time of the Compact Muon Solenoid.

The time stamp behavior of the looped channels is summarized in the ridge plot 5.19. In addition to channel 12, almost 26% of channels show time bin drift. All channels that experienced bin drift are highlighted. Under close examination, the time bin drift happens at different time spans.The labels at each

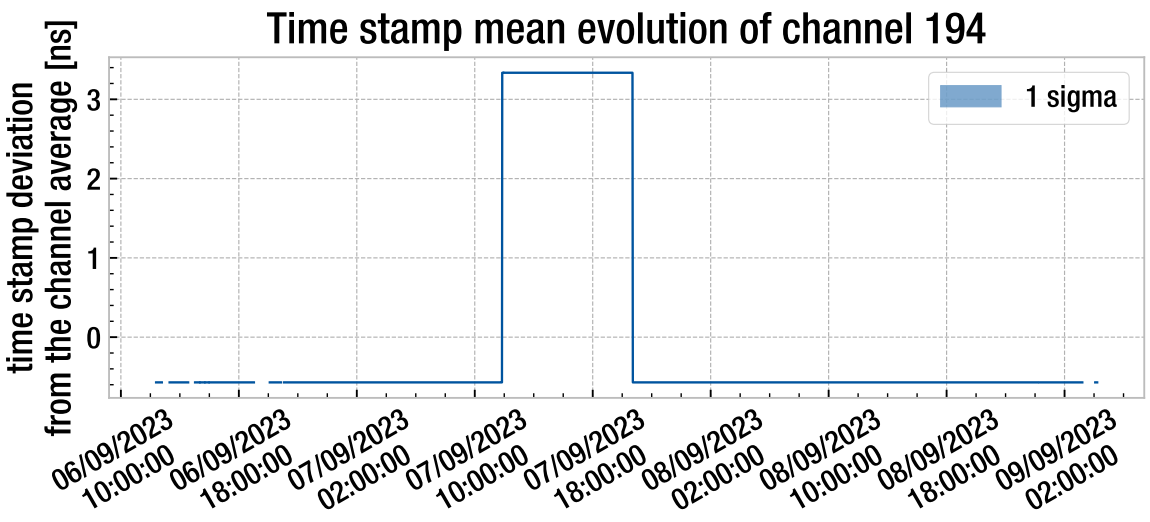

Figure 5.18: A plot depicting the ten-second time stamp recorded for channel 194. The x-axis describes the time of the measurement, and the y-axis shows the deviation of the time stamp mean from channel average. The data was measured by OBDT theta.

end of the signals in the plot indicate the originating channel for the average time stamps. It's also evident from the plot that only half of the connected looped channels registered hits, as the remaining half functioned as sources for the test pulses. Moreover, one front-end connector of the On-Board Drift Tube (OBDT) theta was intentionally left unconnected.

Observing the full picture of the time stamp evolution over the whole 4-day period shows an undisputed stability of the time digitization system. The data show that OBDT theta more than exceeds the 1.4 ms stability goal set by the duration of the DT system calibration[35]. Nevertheless an example of channels 171 and 194 shows that OBDT theta experiences single channel upsets. Therefore, during detector operation the system needs monitoring to ensure that the recorded data describes a muon flying through a drift tube.

Measurements of OBDT theta TDC time stability keep the channel naming convention introduced in 4.3. Ones connected to the front-end boards are called front-end channels and the other channels are called looped channels (Figure 4.4). The more complex information of front-end channels is shown in Figure 5.20 and 5.21. Although the heat maps do not allow distinguishing between the front-end channels, they show that all channels experience the same behavior.

Comparing the channels connected to the front-end board requires picking out time stamps from only one test pulse path. The process decreases the total statistics of the recorded hits, but allows comparing the front-end with looped channels. Taking a closer look at Figure 5.20 shows that the mean of the front-end channels stays within one time bin over the first day of the measurement. Around 16:20 many front-end channels experience a noise spike smaller than the size of one time bin (0.78 ns).

Similarly to the looped channels the front-end channels also show exceptional

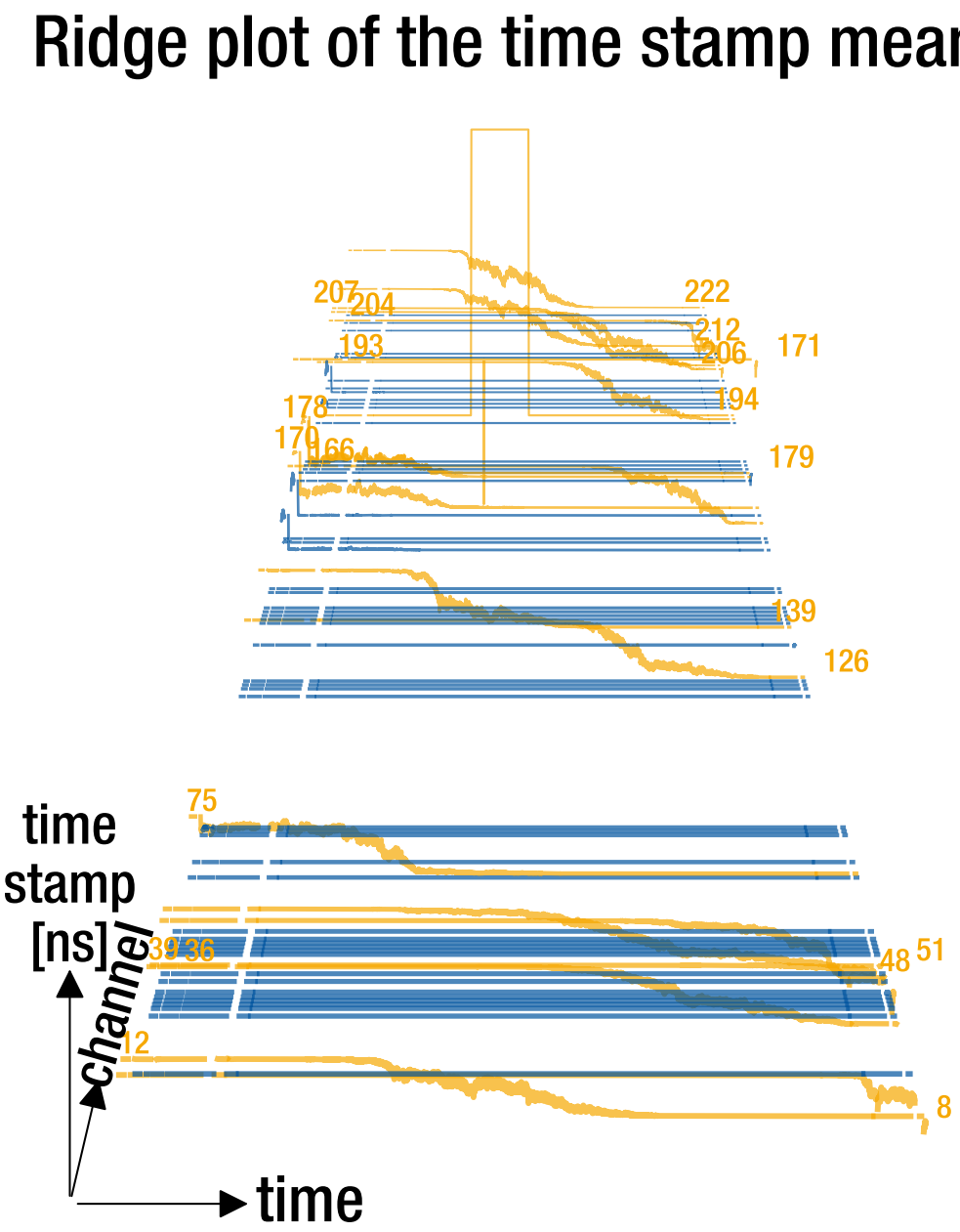

Figure 5.19: A ridge plot demonstrating the time stamp stability of OBDT theta. The x-axis describes the time coordinate, the y-axis a time stamp mean computed over 10 seconds, and the z-axis the channel number. The highlighted channels exhibit either time bin jumps or time bin drift.

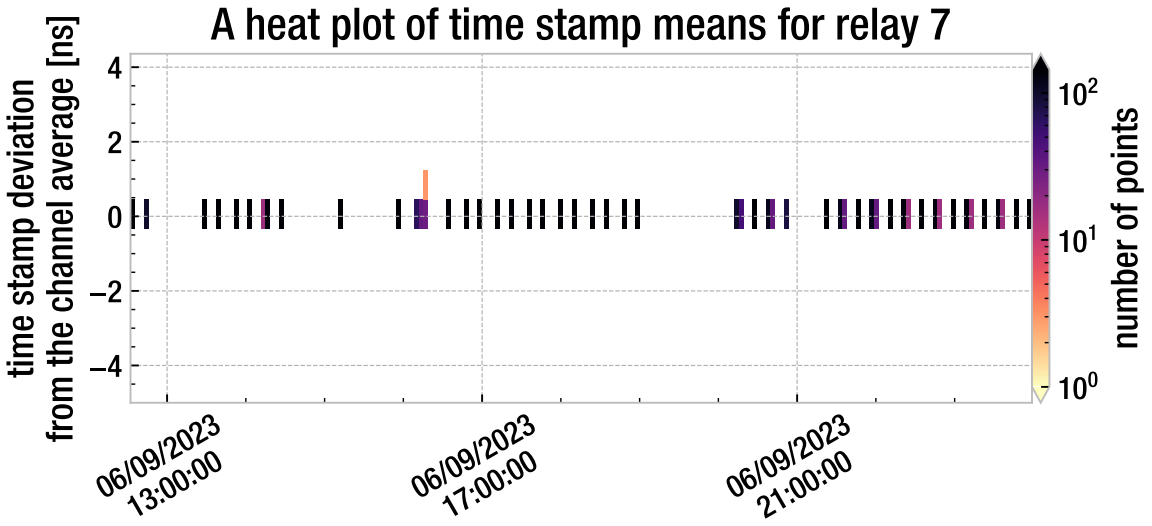

Figure 5.20: A heat map of OBDT theta channels connected to a front-end board. The x-axis describes the time of the measurements, the heat maps also show the timestamp value on the y-axis. The color map describes the number of hits recorded in a specific time coordinate. The test pulses sent to the front-end board came through the seventh relay.

stability. During the first day only a single measurement showed a time stamp distribution not wider than one bin. During the larger gaps around 13:00, 15:00, 15:45, 19:30, and 21:00 the monitoring of OBDT theta did not collect data.
Figure 5.21 especially, illustrates the increased noise of the front-end channels. A less noisy period starts after 6:36 lasting almost until 19:12. Examining the region around the horizontal 0 ns mark, the bulk of time stamp means stays within one time bin of the day average mean. The general trend of all channels shows a time bin drift towards later times. An almost 3 ns time bin jump happens shortly before 22:12. Channels 24 to 29 experience the time bin jump (see appendix A). The other front-end channels remain constant.
During the second to last day of measurements, the noise from the front-end channels increased. A behavior expected considering the collected radiation dose of the electronics. The time stamp distribution shows a time bin drift in progress as the number of hits in the upper bin changes from around 2000 to around 300. The opposite happens for the lower bin. Depending on the closed relay of the multiplexer all front-end channels show time bin drift similar to one shown in 5.17. The time bin jump towards the end of the measurement shows another single event upset caused by the radiation environment. Adding the front-end channels 24 through 29 to looped channels 194 and 171 results in 9% of all channels experiencing multiple minute effects of the radiation environment.
The time bin jump present in the jitter histogram also explains the types of distribution described by Figure 5.9. The lower peak of the distribution comes from a time bin jump just like in the time stamp heat map 5.21.

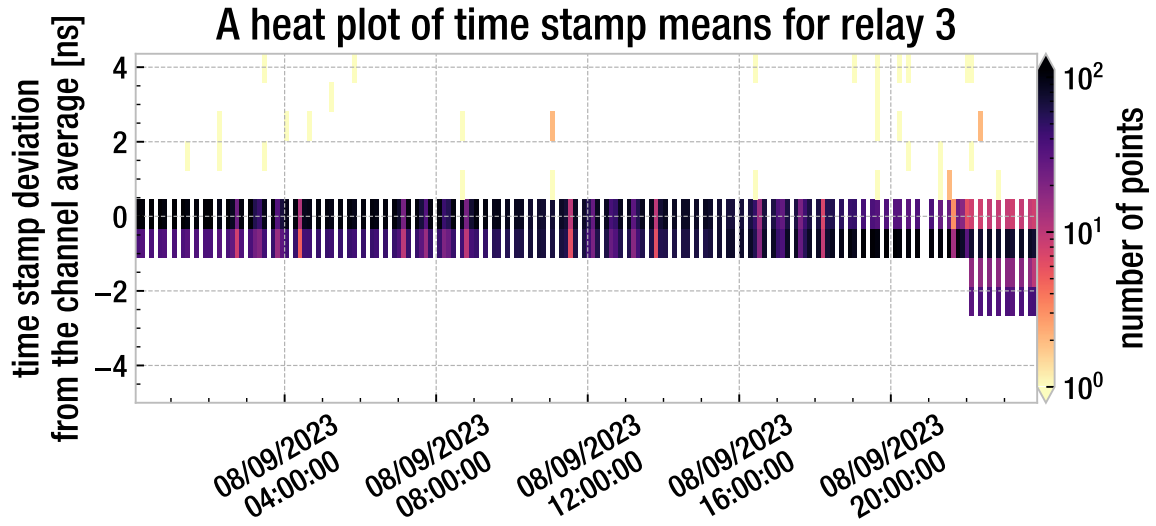

Figure 5.21: A heat map of OBDT theta channels connected to a front-end board. The measurement time is shown on the x-axis, and the y-axis describes the deviation time stamp mean from the channel average of the third measurement day. The test pulses sent to the front-end board passed through the third relay.

The general outcome of the stability examination of OBDT theta shows satisfactory performance of front-end channels. As the most important result of the measurement, time stamps recorded through these channels under irradiation remain stable over an entire day. This result more than exceeds the minimum stability requirement of 1.4 ms [35]. Next 44% of the front-end and 9% of all channels experience a time bin jump because of the radiation environment the electronics experienced. Since the front-end channel jumps occur in all relay configurations, they have to originate from the front-end boards. By contrast, the looped channel time bin jumps have to originate in the OBDT FPGA. The looped channels show stability of the field programmable gate array up to irradiation dose of 35 Gy. Over the four day data taking, only 26% of the channels experienced time bin drift. The magnitude of the drift amounted to at most 1.56 ns.

5.3 Hit rate and detection efficiency of On-Board Drift Tube electronics

Expanding on the work of the Slice Test presented in section 3.4, this thesis examines the efficiency of OBDT phi under higher rates averaging 28 Hz/cm^2 for OBDT phi. Simulating almost 60% of the 50 Hz/cm^2 rates expected at High-Luminosity LHC, the OBDT phi and its testing system are expected to handle these rates [4]. The slow control noise of 1 MHz allowed looking for OBDT phi transmission limits. The efficiency measurements of OBDT phi involved activating an increasing number of channels and sending test pulses (section 4.1). Additionally, the tests at the CERN high energy accelerator mixed field facility

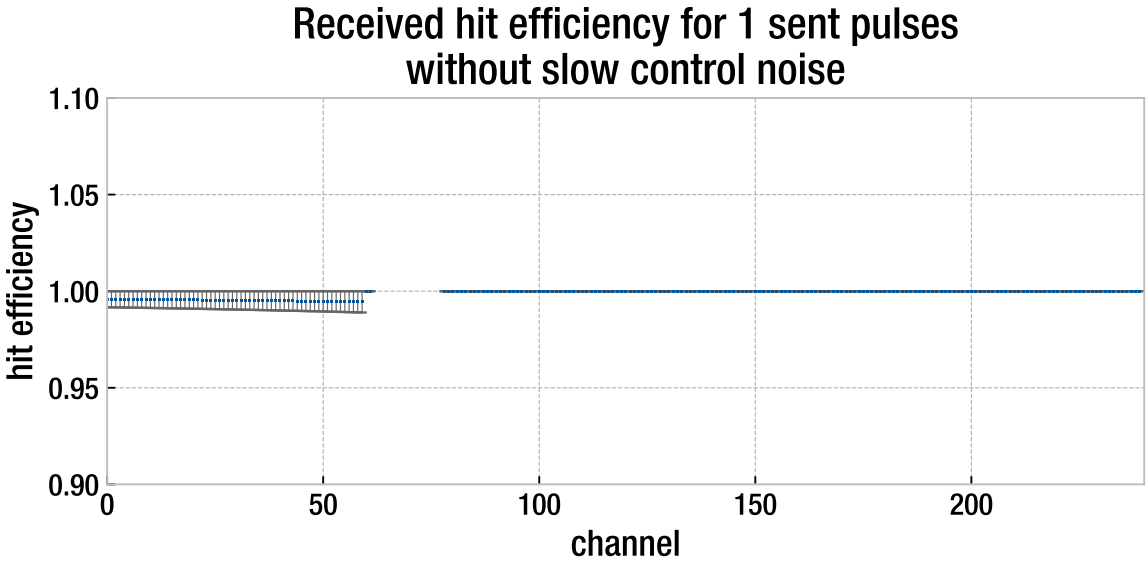

Figure 5.22: A scatter plot showing the test pulse detection efficiency of OBDT phi channels. The x-axis describes the channel number and the y-axis shows the efficiency. The measurement did not include the noise from the slow control. Points at a y-value of zero come from a disconnected cable, and the data were recorded without the front-end noise.

examined the reliability of OBDT theta under a high irradiation environment. During irradiation, the testing software monitored the number of unregistered hits (see section 4.3).

In both cases of hit rate and efficiency measurements, the On-Board Drift Tube electronics is expected to record all hits generated by the test pulse system. In the examination of OBDT phi this translates to all channels reaching the efficiency of one. In contrast , OBDT theta measurements expect to record 0 missing hits across the entire measurement period and across all channels.

The efficiency scatter plot in Figure 5.22 shows efficiency close to one for all channels. Only one sixth of the channels miss one hit out of around 200. Because one front-end cable did not connect to a front-end board channels 62 through 78 do not appear in the efficiency plot. The errors are taken to be binomial leading to the efficiencies of 0 and 1 to have no errors as intended. Due to the measurement method, higher channel numbers have smaller statistics supporting their efficiency.

Data show that OBDT phi can forward up to 224 hits within almost one bunch crossing without substantial data losses. Because most OBDT phi will not use all front-end connectors, the plot proves that they will be capable of handling 224 hits in one second intervals. Considering that a muon track usually leaves three or four hits in a muon chamber super layer the measurement shows that OBDT phi could handle between around 60 muons passing through the super layer. The calculation also assumes that the muons each pass through different drift tube stack within 28 ns.

After adjusting the measurement method by including masking of the front-end boards, OBDT phi significantly lose efficiency (Figure 5.23). The loss arises

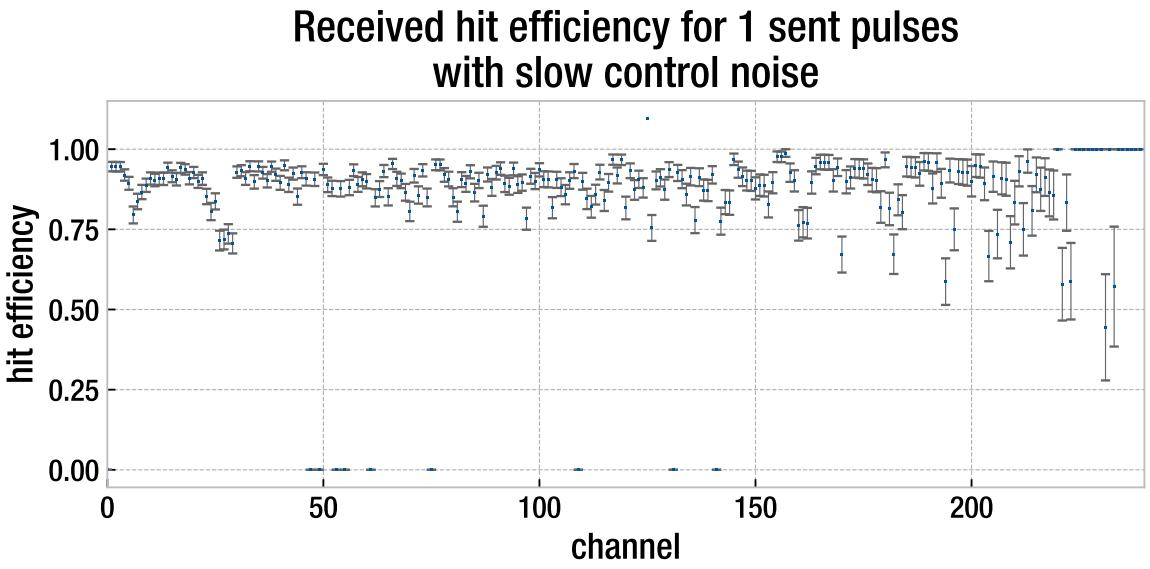

Figure 5.23: A scatter plot showing the test pulse detection efficiency of OBDT phi channels. Channel numbers are describe by the x-axis and the channel efficiency is on the y-axis. The measurement included noise from the slow control. The points at a y-value of zero come from filtering of noisy channels.

from ten noisy channels resting at zero efficiency because they were filtered out from the data. The distribution changes to a more randomly distributed behavior. Many channels retain 90% efficiency, and the channels with higher numbers reach 100%. The lowest efficiency of about 44% is recorded by the channel 231. In total, 16 channels exhibit efficiency below 75%. Finally, channel 125 reaches efficiency higher than one because it experienced low rate noise. The noise is also visible in Figure 5.3.

Histogramming the efficiencies gives an a better overview of the observed time stamp losses (Figure 5.24). Around 70% of the channels still retain efficiency above 90%. The histogram also clearly shows the 10 noisy channels and channel 125 which experienced low amount of noise, reaching efficiency higher than one.

Observing the efficiency histogram, the noisy channels saturated the transmission capabilities of the experimental setup. Caused by the slow control, the ten channels collectively introduced close to 1 MHz of noise. The number comes from the 100 kHz frequency used for the slow control of the front-end boards (FEBs) multiplied by nine noisy channels. The plot describes that either OBDT phi or the testing board HTG-940 cannot cope with the noise and extra hits. Comparing the noise rate to the expected rate of 50 Hz/cm^2, which translates to 1.7 MHz per MB3 chamber section, the setup cannot handle 56% of the 50 Hz/cm^2 rate without losing data.

The rates created at CERN high energy accelerator mixed field facility did not reach as high as On-Board Drift Tube electronicsphi tests. Therefore, the detection efficiencies were much higher. To see the small inefficiencies, two-dimensional histograms show the number of missing hits in ten seconds over

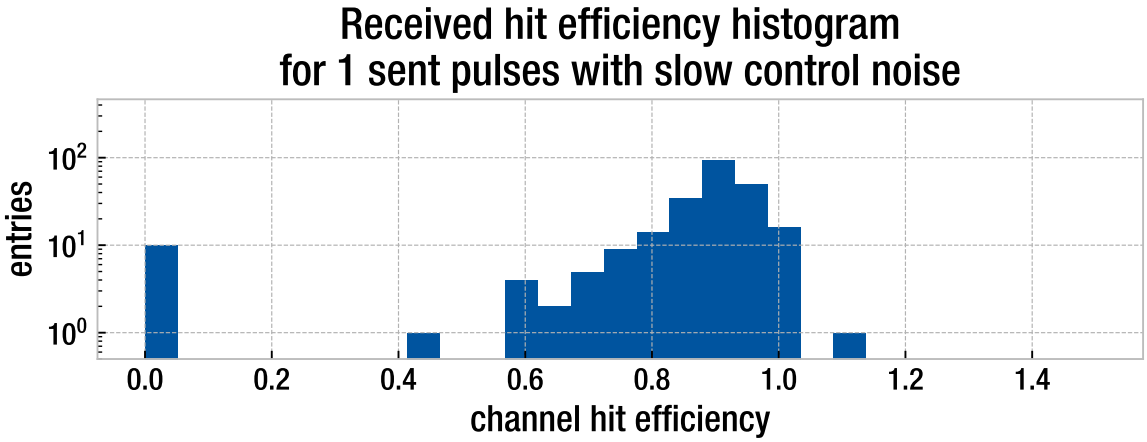

Figure 5.24: A histogram that displays the efficiencies of OBDT phi channels. The efficiency value is on the x-axis and the number hits in a given bin on a logarithmic y-axis. The entries at 0 efficiency originate from noisy channels and the single entry beyond one belongs to one channel with low noise.

the whole measurement campaign (Figures 5.25, 5.26, 5.27, and 5.28).

The first-day measurements shown in Figure 5.25, record at most eleven missing hits in the front-end channels (explicitly 0, 3, 4, 5, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, and 35). The first set of missing hits appears between 15:00 and 19:00. The second set starts at 20:00 and ends around 20:45. The third and final group of missing hits lasts no longer than 15 minutes starting at 21:00.

Because the number of missing hits is lower than one percent of the total test pulse hits issued through the front-end board, the efficiency is excellent. The measurement was off during the wider gaps between bins with missing hits. The measured inefficiencies originate from incorrectly timed switching. Because the relays switched after and not before the measurement ended, the first pulses issued through the next line did not reach the FPGA pins. The inefficiencies disappear after an adjustment of the testing procedure.

Figure 5.26 shows almost no missing hits. The single missing hit in each channel occurred about 15 minutes before 15:00. The rest of the measurements did not experience any hit losses.

Considering that the simulated hit rate during the test reached 291 Hz per channel, the hit rate OBDT theta handled reaches more than 26 kHz. The calculation involves the 291 Hz base rate and multiplying it by 16 front-end and 74 looped channels. The data set a new boundary on the hit rate OBDT theta can handle in a radiation environment.

Measurements on the third day show missing hits in channels connected to the front-end board (Figure 5.27). Starting shortly after 20:15 in a periodic sequence of about eleven minutes, the pattern continues until the end of the day. The channels miss 100% of issued hits. In addition to the missing hits of the front-end channels, all monitored channels record a missing hit around 21:30.

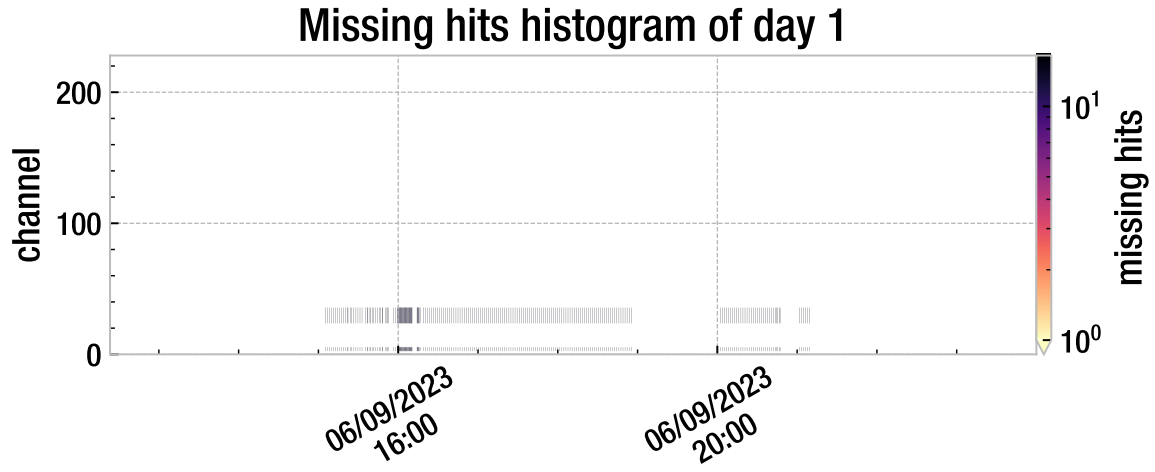

Figure 5.25: A two-dimensional histogram depicting the number of missing hits as a logarithmic color hue. The y-axis describes the channel number, and the measurement time shows on the x-axis. The plot shows the data from the first day of the measurement campaign. OBDT theta recorded the data.

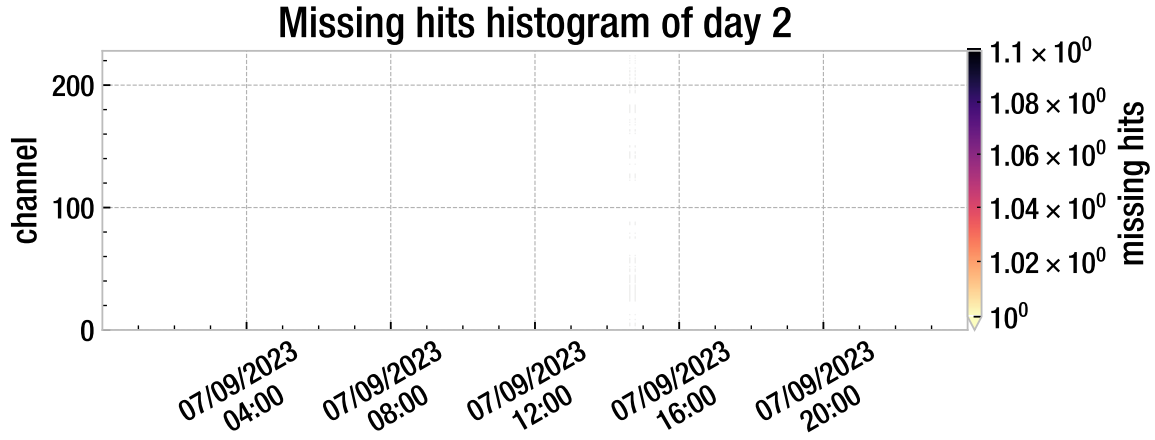

Figure 5.26: A two-dimensional histogram depicting the number of missing hits as a logarithmic color hue. The y-axis describes the channel number, and the measurement time shows on the x-axis. The plot shows the data from the second day of the measurement campaign. OBDT theta recorded the data.

The missing hits recorded at the end of the third day during the measurement campaign come from an implemented testing procedure. During this time none of the test pulse relays were closed, so no test pulses reached the front-end boards. Apart from these planned missing hits, OBDT theta missed only a single hit around 21:30. Adding to the total of previous measurements, the histogram 5.27 expands the efficiency of the OBDT theta.

The final recorded day of the irradiation campaign registers missing hits starting from 10^2 and reaching more than 10^5 missing hits in one ten-second mea-

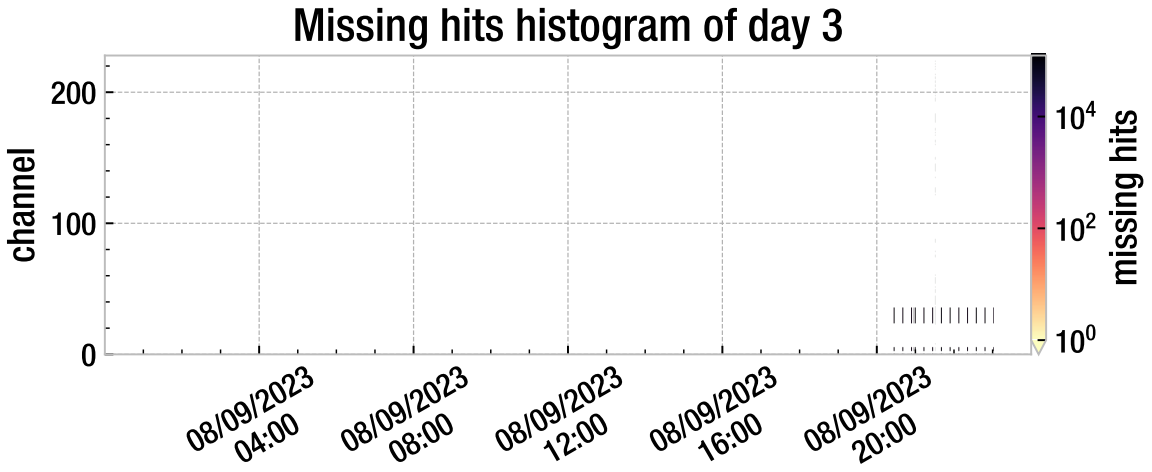

Figure 5.27: A two-dimensional histogram depicting the number of missing hits as a logarithmic color hue. The y-axis describes the channel number, and the measurement time shows on the x-axis. The plot shows the date from the third day of the measurement campaign. OBDT theta recorded the data.

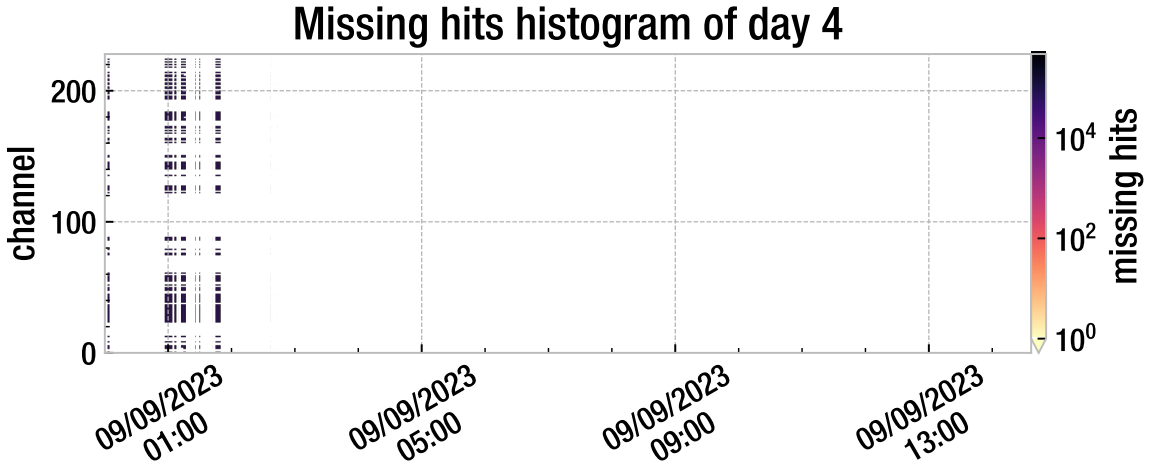

Figure 5.28: A two-dimensional histogram depicting the number of missing hits as a logarithmic color hue. The y-axis describes the channel number, and the measurement time shows on the x-axis. The plot shows the date from the fourth day of the measurement campaign. OBDT theta recorded the data.

surement. In Figure 5.28, the first instance appears directly after midnight and the net groups of missing hits start shortly before 1:00 and end after 1:45. Both the looped and the front-end channels experience inefficiencies.

The final missing hits arise from restarting procedures undertaken to reestablish the communication with the OBDT theta. Shortly before 2:00 during the fourth day measurement irreversibly shut down. Because the communication was not established all of the monitored channels experienced hit losses. The

channels miss 100% of the hits, similarly to the end of the previous day. In total OBDT theta survived up to 35 Gy, 70-times the High-Luminosity LHC dose.

The efficiency measurements of OBDT phi show promising results. The tests at INFN Legnaro show that OBDT phi can handle processing up to 224 simultaneous hits in relaxed conditions. With no background noise and one second between each test pulse firing, OBDT phi practically registers all hits.
High rate tests were able to find the transmission limit of the experimental setup. With background hit rate close to 1 MHz, the firmware of OBDT phi or the HTG-940 were not capable of recording issued hits. Compared to the expected benchmark of 1.7 MHz coming from the 50 Hz/cm^2 rate, the firmware does not pass the test [4]. This result serves as an excellent reason to perfect the OBDT FPGA firmware, so by the time High-Luminosity LHC starts, the On-Board Drift Tube electronics (OBDT) transfer all timestamps.

Efficiency tests of OBDT theta display positive results as well. Measurements at CERN high energy accelerator mixed field facility display that only two hits per monitored channel are attributable to the electronics inefficiency. A result more impressive when the radiation operational environment is taken into account. The other observed missing hits can be attributed to errors in the testing procedure, intentional multiplexer settings, or OBDT theta restarting procedures.
Due to the testing setup limitations, the test of OBDT theta did not aim to find the transmission limit of the system. Nevertheless, the tests at CERN high energy accelerator mixed field facility proved that OBDT theta can handle more than 26 kHz average hit rates with insignificant efficiency loss. An important contribution of the measurements at CERN high energy accelerator mixed field facility is the test of electronics in the radiation environment. OBDT theta survives radiation dose of 35 Gy, 70-times the expected 0.5 Gy [22]. Consequently, the result shows that the OBDT theta is very likely to survive entire High-Luminosity LHC operations. The irradiation shows little influence on the hit recording capabilities of On-Board Drift Tube electronics (OBDT) theta. Passing this benchmark is an important milestone in the electronics verification.

Chapter 6

Jitter, timing stability, and pre-production steps of On-Board Drift Tube electronics

This thesis has focused on the Phase 2 upgrade of the CMS muon chamber readout electronics. As the electronics production approaches, tests of the developed On-Board Drift Tube electronics (OBDT) need to ensure their stability and reliability. Crucially, the tests need to emulate stresses experienced over the whole lifespan of the electronics. This work has examined the performance of test pulse and time-digitization systems of the On-Board Drift Tube electronics.

6.1 OBDT experience timing and jitter performance

Time-to-digital converter stability tests at CERN high energy accelerator mixed field facility of OBDT theta show outstanding performance. 79% channels stay stable longer than the 1.4 ms benchmark [35], drifting less than 0.78 ns over the four day measurement and after receiving 35 Gy. Only 26% of channels experience time-bin drift of up to 1.56 ns. The 9% of channels affected by single event upsets highlight the importance of detector performance monitoring.
A critical area of investigation was the new readout jitter. Analyzing timestamp distributions recorded by both On-Board Drift Tube electronics types showed that the phi version experiences jitter slightly larger than seen in the legacy hardware. The measured average standard deviation of each timestamp distribution reached 1.37 ± 0.33 ns compared to the expected 1 ns [35]. Next, the jitter analysis of OBDT theta show exceptionally low jitter of 0.32 ± 0.13 ns highlighting the timing accuracy of the readout electronics and their test pulse system.
Additionally, the jitter analysis examined the spread of timestamp distributions. Included in an experimental setup OBDT theta demonstrated a much narrower spread of timestamp distributions, reaching less than 10 ns. This spread is narrower than the spread recorded by OBDT phi, exceeding 25 ns.
The measurements conducted to test OBDT phi revealed a drop in the ef-

ficiency of the transmission setup when subjected to 28 Hz/cm^2 background hit rate. Without the background hit rate, the experimental setup reached detection efficiency really close to 100%. In a different measurement campaign OBDT theta demonstrated immaculate efficiency (almost indistinguishable from 100%). The measurements also present that the tested OBDT theta survived an irradiation dose of 35 Gy, showing it will very likely survive the High-Luminosity LHC irradiation dose of 0.5 Gy and perform without problems [22].

6.2 Next steps

Looking ahead, future work should focus on understanding discrepancies in timestamp distributions between the two On-Board Drift Tube electronics versions. This difference warrants further investigation to determine the differences between the two versions.
In terms of necessary improvements, the OBDT phi measurements point to the experimental setup. The explored transmission limit of 28 Hz/cm^2 highlights the need to improve the firmware towards the design goal of 50 Hz/cm^2 [4].
Lastly, future tests should expand the high rate measurements to OBDT theta. These tests should include an improved experimental setup with more precise hit emulation methods and investigate the high-rate capabilities of OBDT theta. In a similar manner, the time-to-digital converter stability test carried out under irradiation needs to be repeated for OBDT phi.

Acronyms

LHC Large Hadron Collider

CMS Compact Muon Solenoid

ATLAS A Torodial LHC Apparatus

ALICE A Large Ion Colider Experiment

LHCb Large Hadron Colider for beauty

CERN Conseil Européen pour la Recherche Nucléaire

FPGA field programmable gate array

MB Muon chamber Barell

CSC Cathode-Strip Chamber

RPC Resistive Plate Chamber

HTG HiTech Global

CO_2 carbon dioxide

$PbWO_4$ lead tungstate

DT drift tube

OBDT On-Board Drift Tube electronics

HCAL hadronic calorimenter

ECAL electromagnetic calorimeter

lpGBT low-power gigabit transciever

VTRx+ Versatile Transciever Link plus

TDC time-to-digital converter

ASIC application-specific integrated circuit

FEB front-end board

SCA slow control adapter

CHARM CERN high energy accelerator mixed field facility

DNL differential non-linearity

IC integrated circuit

LVDS low-voltage differential signal

ROB read-out board

TRB trigger board

INFN Istituto Nazionale di Fisica Nucleare

I^2C inter-integrated circuit

MAD Multichannel Amplifier-Discriminator

Appendix A

Complementary plots

The following plots supplement data in the previous sections of the thesis. They range from irradiation dose plots to scatter plots of time stamp distributions.

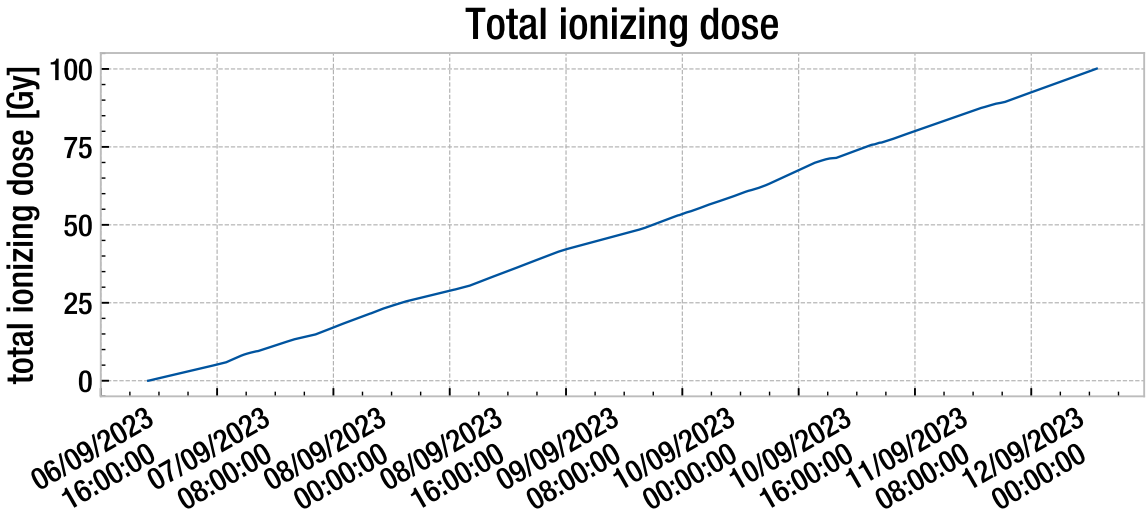

Figure A.1: The plot describes the measurement of total registered radiation dose delivered during the measurements at CERN high energy accelerator mixed field facility. OBDT theta malfunctioned and stopped working at the beginning of the 9th of September after receiving 35 Gy. The x-axis describes the time, and the y-axis describes the total ionizing dose.

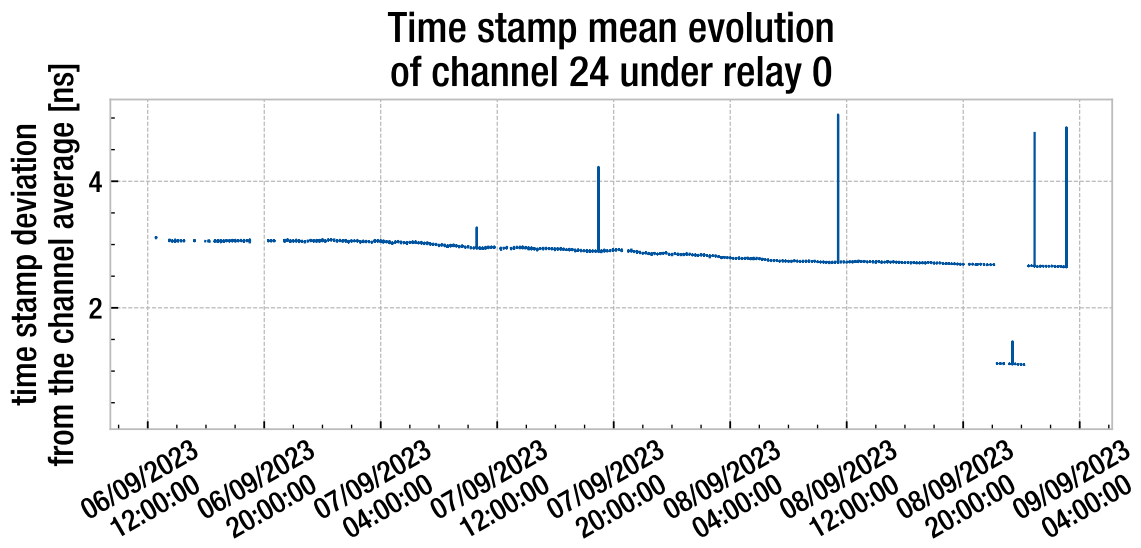

Figure A.2: A plot of the channel time stamp mean evolution measured by OBDT theta. The data shown in the plot have been heavily filtered. An important feature of the plot is the time bin jump on the right side of the plot. The x-axis descrbes the time of the measurement and the y-axis the time stamp distribution mean measured over ten seconds. The data originate from channel 24 under relay 0.

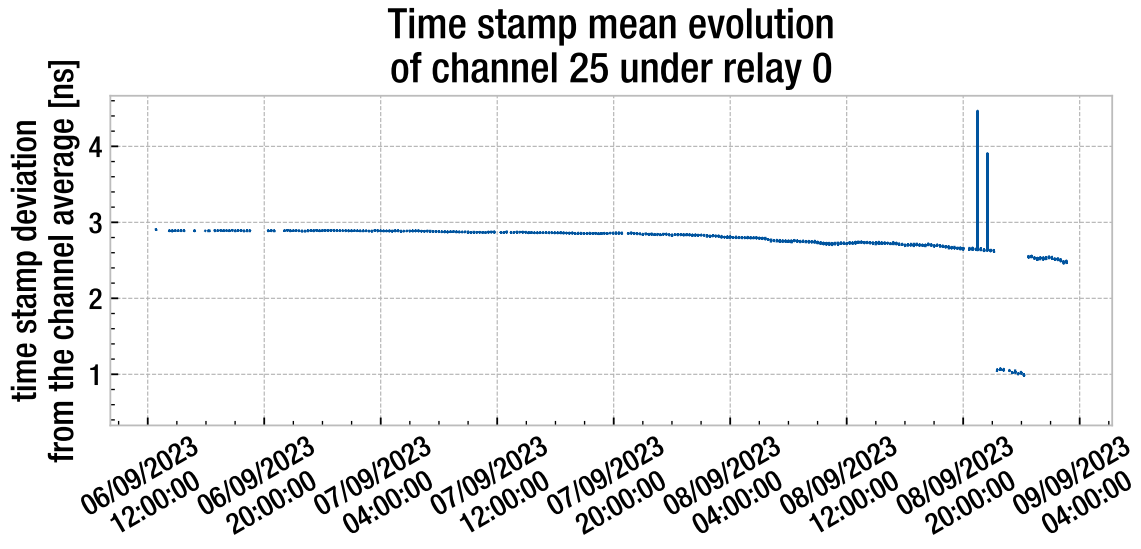

Figure A.3: A plot of the channel time stamp mean evolution measured by OBDT theta. The data shown in the plot have been heavily filtered. An important feature of the plot is the time bin jump on the right side of the plot. The x-axis descrbes the time of the measurement and the y-axis the time stamp distribution mean measured over ten seconds. The data originate from channel 25 under relay 0.

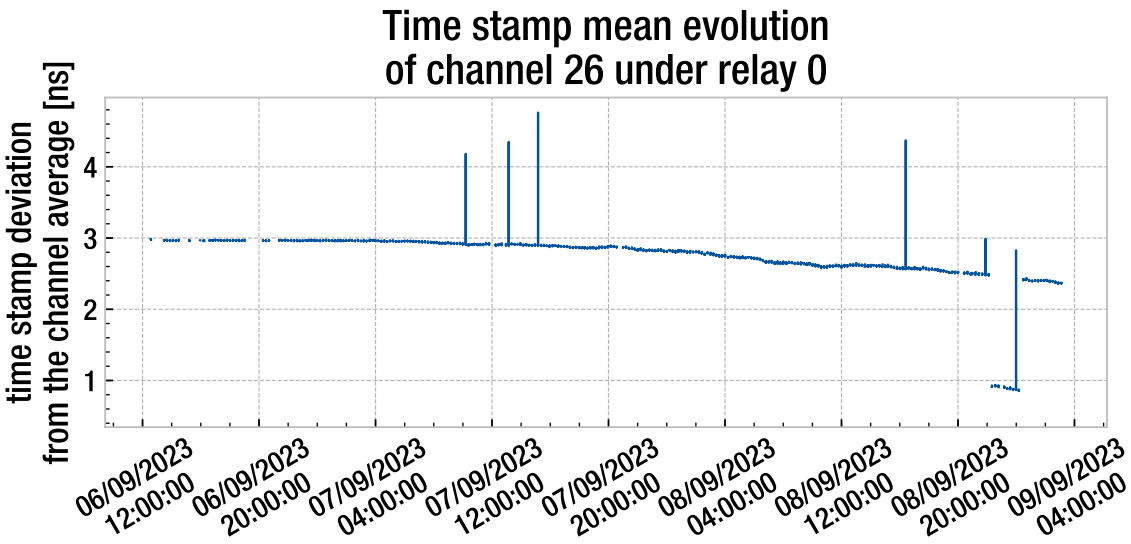

Figure A.4: A plot of the channel time stamp mean evolution measured by OBDT theta. The data shown in the plot have been heavily filtered. An important feature of the plot is the time bin jump on the right side of the plot. The x-axis descrbes the time of the measurement and the y-axis the time stamp distribution mean measured over ten seconds. The data originate from channel 26 under relay 0.

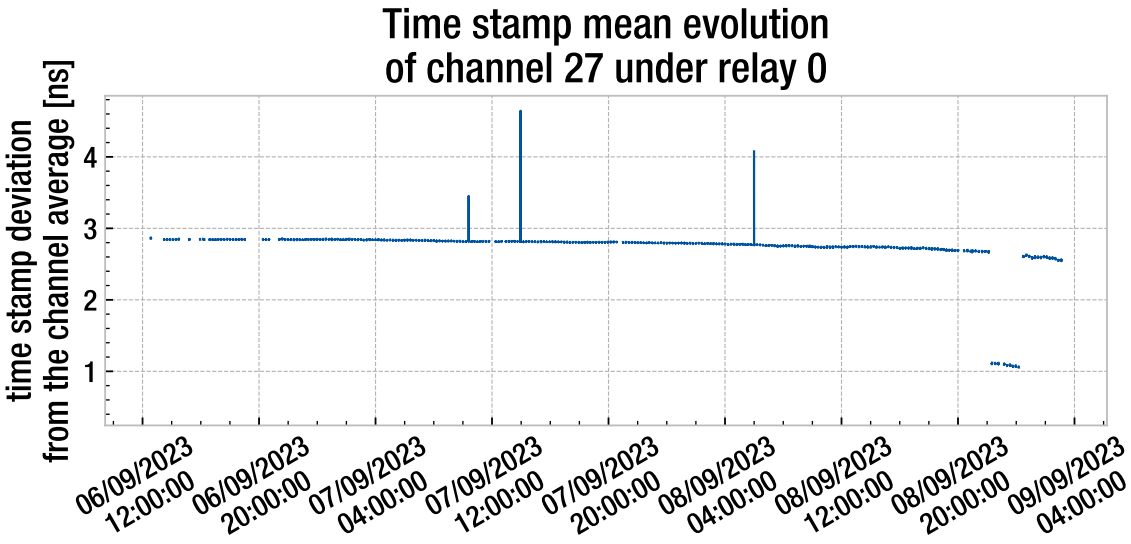

Figure A.5: A plot of the channel time stamp mean evolution measured by OBDT theta. The data shown in the plot have been heavily filtered. An important feature of the plot is the time bin jump on the right side of the plot. The x-axis descrbes the time of the measurement and the y-axis the time stamp distribution mean measured over ten seconds. The data originate from channel 27 under relay 0.

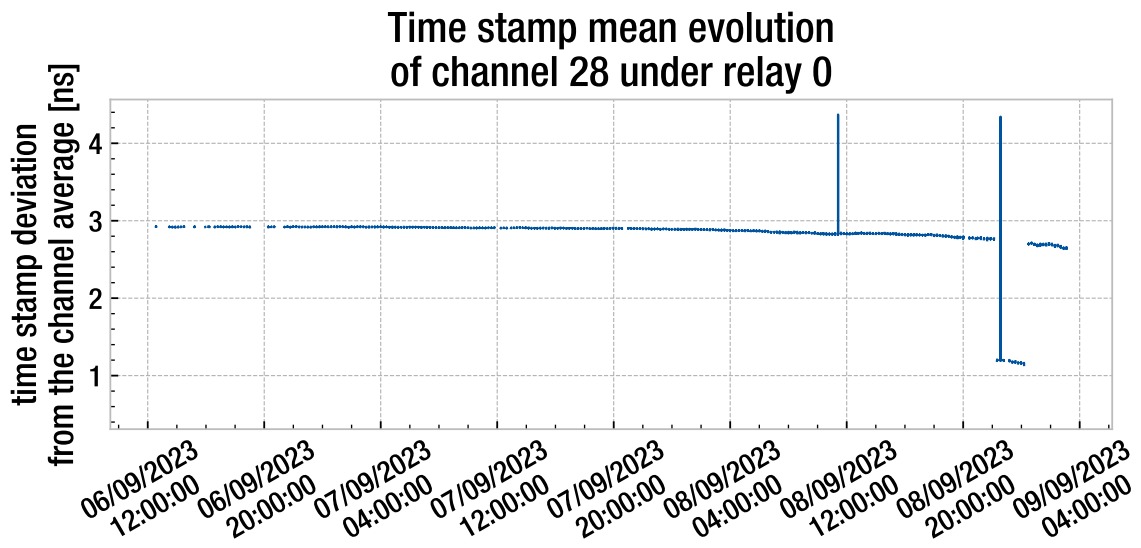

Figure A.6: A plot of the channel time stamp mean evolution measured by OBDT theta. The data shown in the plot have been heavily filtered. An important feature of the plot is the time bin jump on the right side of the plot. The x-axis descrbes the time of the measurement and the y-axis the time stamp distribution mean measured over ten seconds. The data originate from channel 28 under relay 0.

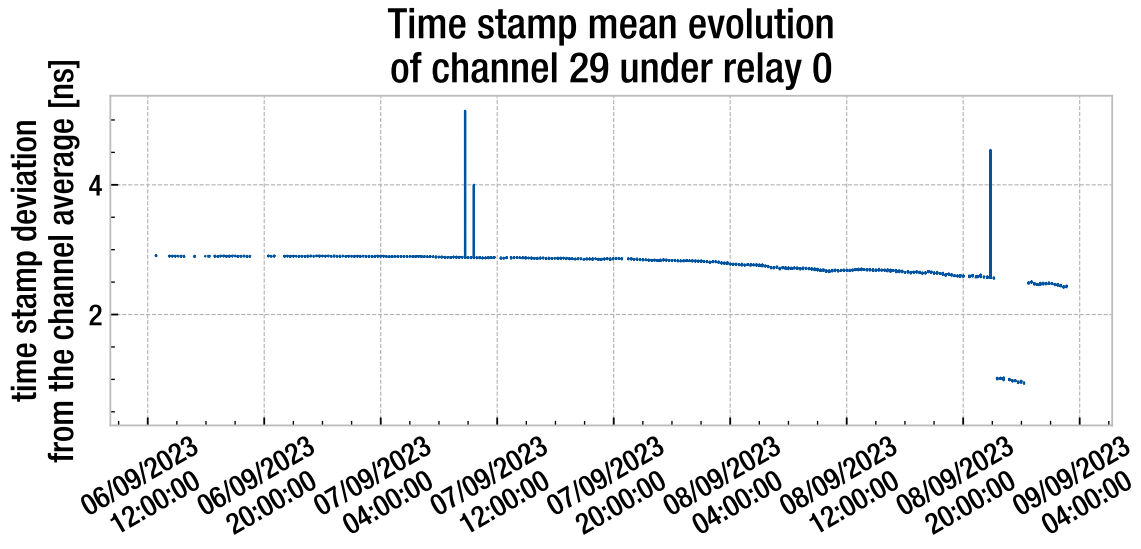

Figure A.7: A plot of the channel time stamp mean evolution measured by OBDT theta. The data shown in the plot have been heavily filtered. An important feature of the plot is the time bin jump on the right side of the plot. The x-axis descrbes the time of the measurement and the y-axis the time stamp distribution mean measured over ten seconds. The data originate from channel 29 under relay 0.

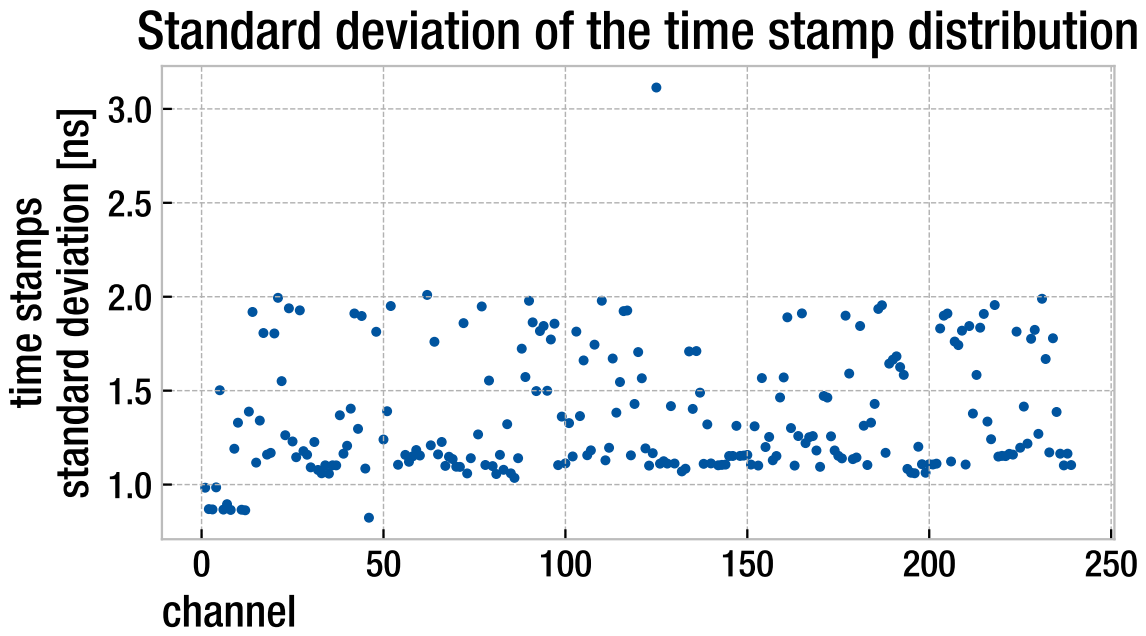

Figure A.8: The figure shows the timestamps distribution standard deviations for OBDT phi. The x-axis describes the channel number, and the y-axis depicts the magnitude of the deviation in nanoseconds.

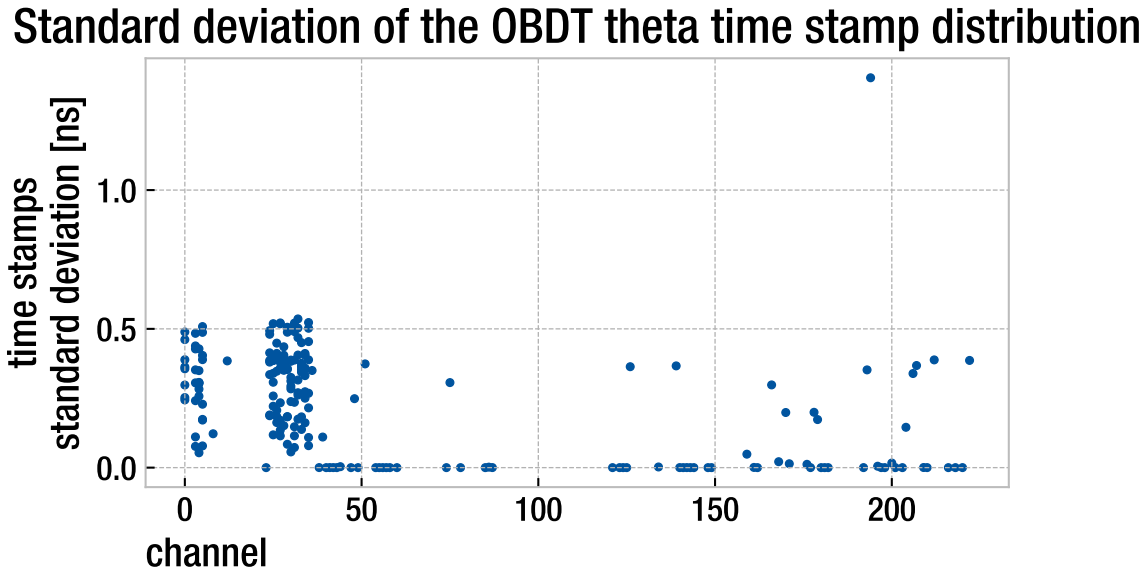

Figure A.9: The figure shows the timestamps distribution standard deviations for OBDT phi. The x-axis describes the channel number, and the y-axis depicts the magnitude of the deviation in nanoseconds.

Bibliography

[1] S. Weinberg. “The making of the Standard Model”. In: *The European Physical Journal C* 34.1 (2004), 5–13. DOI: 10.1140/epjc/s2004-01761-1. URL: http://dx.doi.org/10.1140/epjc/s2004-01761-1.

[2] Lyndon Evans and Philip Bryant. “LHC Machine”. In: *Journal of Instrumentation* 3.08 (2008), S08001. DOI: 10.1088/1748-0221/3/08/S08001. URL: https://dx.doi.org/10.1088/1748-0221/3/08/S08001.

[3] O.; et. al Aberle. *High-Luminosity Large Hadron Collider (HL-LHC): Technical design report*. CERN Yellow Reports: Monographs. Geneva: CERN, 2020, pp. 1–11,345. DOI: 10.23731/CYRM-2020-0010. URL: https://cds.cern.ch/record/2749422.

[4] CMS Collaboration. *The Phase-2 Upgrade of the CMS Muon Detectors*. Tech. rep. Geneva: CERN, 2017. URL: https://cds.cern.ch/record/2283189.

[5] Tatsumi Aoyama et al. “Tenth-order electron anomalous magnetic moment: Contribution of diagrams without closed lepton loops”. In: *Phys. Rev. D* 91 (3 2015), p. 033006. DOI: 10.1103/PhysRevD.91.033006. URL: https://link.aps.org/doi/10.1103/PhysRevD.91.033006.

[6] Mark Thomson. *Modern particle physics*. New York: Cambridge University Press, 2013. ISBN: 978-1-107-03426-6. DOI: 10.1017/CBO9781139525367.

[7] Wikimedia Commons. *Standard Model of Elementary Particles*. 2019. URL: https://w.wiki/7pnJ.

[8] H. Kolanoski and Wermes N. *Teilchendetektoren*. Heidelberg: Springer Spektrum Berlin, 2016. ISBN: 978-3-662-45350-6. DOI: 10.1007/978-3-662-45350-6.

[9] ATLAS Collaboration. “Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC”. In: *Physics Letters B* 716 (2012), 1–29. DOI: 10.1016/j.physletb.2012.08.020. URL: http://dx.doi.org/10.1016/j.physletb.2012.08.020.

[10] CMS Collaboration. “Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC”. In: *Phys. Lett. B* 716 (2012), p. 30. DOI: https://doi.org/10.1016/j.physletb.2012.08.021. URL: https://www.sciencedirect.com/science/article/pii/S0370269312008581.

[11] CERN. *LHC long term schedule*. 2022. URL: http://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm.

[12] Maximilien Brice. “Aerial View of the CERN taken in 2008.” 2008. URL: https://cds.cern.ch/record/1295244.

[13] *LHC Guide*. 2017. URL: https://cds.cern.ch/record/2255762.

[14] CMS Collaboration. *Detector Drawings*. 2012. URL: https://cds.cern.ch/record/1433717.

[15] The CMS Collaboration. “The CMS experiment at the CERN LHC”. In: *Journal of Instrumentation* 3.08 (2008), S08004. DOI: 10.1088/1748-0221/3/08/S08004. URL: https://dx.doi.org/10.1088/1748-0221/3/08/S08004.

[16] Candan Isik. *Phase 1 Upgrade of the CMS Hadron Calorimeter*. Tech. rep. Geneva: CERN, 2022. DOI: 10.1016/j.nima.2022.167389. URL: https://cds.cern.ch/record/2810162.

[17] Michael Sowa. "Tests of Data Acquisition System and Detector Control System for the Muon Chambers of the CMS Experiment at the LHC". PhD thesis. Aachen: RWTH Aachen University, 2009, 23–61.

[18] F. R. Cavallo et al. *Test of CMS Muon Barrel Drift Chambers with Cosmic Rays*. Tech. rep. Geneva: CERN, 2003. URL: http://cds.cern.ch/record/687871.

[19] Lucas Taylor. "Detecting Muons". In: (2011). URL: https://cms.cern/book/export/html/1203.

[20] F Gonella and M Pegoraro. ""The MAD", a Full Custom ASIC for the CMS Barrel Muon Chambers Front End Electronics". In: (2001). DOI: 10.5170/CERN-2001-005.204. URL: https://cds.cern.ch/record/529411.

[21] "cms frontend". design schematics. 1999.

[22] Rubén García Alía et al. "LHC and HL-LHC: Present and future radiation environment in the high-luminosity collision points and RHA implications". In: *IEEE Trans. Nucl. Sci.* 65.1 (2018), pp. 448–456. DOI: 10.1109/TNS.2017.2776107. URL: http://cds.cern.ch/record/2310128.

[23] Javier Sastre Alvaro. *The OBDT board: A prototype for the Phase 2 Drift Tubes on-detector electronics*. Tech. rep. Geneva: CERN, 2020. URL: https://cds.cern.ch/record/2797780.

[24] lpGBT Design team. *lpGBT Documentation*. 2022. URL: https://cds.cern.ch/record/2809058.

[25] A Caratelli et al. "The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments". In: *JINST* 10.03 (2015), p. C03034. DOI: 10.1088/1748-0221/10/03/C03034. URL: https://cds.cern.ch/record/2158969.

[26] CMS Collabooration. "The VTRx+, an optical link module for data transmission at HL-LHC". In: *PoS* TWEPP-17 (2017), 048. 5 p. DOI: 10.22323/1.313.0048. URL: https://cds.cern.ch/record/2312396.

[27] Microchip Technology Inc. and its subsidiaries. "PolarFire FPGA". In: (2021).

[28] Alvaro Navarro Tobar. *Time Digitization firmware for the new Drift Tubes electronics for HL-LHC*. Tech. rep. Geneva: CERN, 2021. DOI: 10.1109/NSS/MIC44867.2021.9875454. URL: https://cds.cern.ch/record/2798168.

[29] Archie Sharma. *The Phase-2 Upgrade of the CMS Drift Tube (DT) detectors for High Luminosity LHC*. Tech. rep. Geneva: CERN, 2022. URL: https://cds.cern.ch/record/2815418.

[30] Adam Thornton. "CHARM Facility Test Area Radiation Field Description". In: (2016). URL: https://cds.cern.ch/record/2149417.

[31] HiTech Global. "HTG-940: Virtex UltraScale+ ™ QUAD FMC+ Development Platform". In: (2023).

[32] Xilinx. "Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics". In: (2019).

[33] Xilinx. "Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics". In: (2021).

[34] Alvaro Navarro Tobar et al. internal presentation.

[35] CMS Collaboration. "Calibration of the CMS drift tube chambers and measurement of the drift velocity with cosmic rays. Calibration of the CMS Drift Tube Chambers and Measurement of the Drift Velocity with Cosmic Rays". In: *JINST* 5 (2010), T03016. DOI: 10.1088/1748-0221/5/03/T03016. arXiv: 0911.4895. URL: https://cds.cern.ch/record/1223943.

Typeset January 25, 2024